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A biphase shift keying (BPSK), direct sequence, spread spectrum modem for Petite Amateur Navy Satellite (PANSAT).

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The development of a biphase shift keying (BPSK), direct sequence, spread spectrum modem is conducted for the purpose of developing a prototype design to be implemented in Petite Amateur navy Satellite (PANSAT). The design discussion includes the hardware used in the functional realization of a working design. The design itself, encompasses selection of components, and demonstrates through circuit diagrams and waveforms produced that the preliminary operational characteristics of a spread spectrum BPSK modulation scheme for PANSAT have been achieved. Limited performance analysis is conducted through IF loop-back testing and analyzes the demodulator output waveforms providing the proof of concept for the design. The development of the final version operating at the specified radio frequency (RF) is not conducted.

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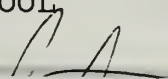
by

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ABSTRACT

The development of a bi-phase shift keying (BPSK), direct sequence, spread spectrum modem is conducted for the purpose of creating a prototype design to be implemented in the Petite Amateur Navy Satellite (PANSAT). The design discussion includes the hardware used in the functional realization of a working design. The design itself encompasses selection of components and demonstrates (through circuit diagrams and waveforms produced) that the preliminary operational characteristics of a spread spectrum BPSK modulation scheme for PANSAT have been achieved. Limited performance analysis is conducted through IF loop-back testing and provides the intermediate and output demodulator waveforms. The development of the final version operating at the specified radio frequency (RF) is not conducted, but the discussion provides proof of concept.

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I. INTRODUCTION

A. GENERAL

Spread spectrum communications systems have become an increasingly important area for research and development. Due to the ever-increasing demands on the available electromagnetic spectrum, there is a growing need for higher data rate, digital communications systems. In some situations it is also desirable to reduce the probability of interference through jamming environments or over crowded radio frequency communications channels. Additionally, others may require a reduced probability of intercept to provide a secure means of transmitting data. Clearly, advances in the area of digital communications are bound by these requirements to produce modulation schemes but, of particular interest in the military, is the creation of communication systems that are robust enough to provide a reliable link in jamming environments. This, coupled with the rapid rise in the number of potential users and the need for systems that can be established rapidly in remote locations, require more sophisticated systems. Such systems can be designed such that their susceptibility to interference is low and their overall performance characteristics are desirable. Spread spectrum communications systems lend themselves to be uniquely suited to meet these demands [Ref.3:p.539].

B. TECHNICAL BACKGROUND

Spread spectrum utilizes a high bit-rate coding sequence to modulate and demodulate the data which is sent over the transmission channel. The use of this coding sequence changes the spectral bandwidth of the modulation scheme and is usually one or two orders of magnitude wider than that of its standard (non-

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spread) counterpart. This unconventional treatment of channel bandwidth appears flagrantly irresponsible with regard to bandwidth conservation. However, the potential interference created on adjacent channel frequencies by the resulting signal, in many instances, is negligible since the resulting signal is at or below the channel noise level. Additionally, the transmitted signal is only detectable by a receiver configured with the identical coding sequence. An added benefit is realized during demodulation whereby, narrow band noise introduced on the channel (jamming) will not interfere with demodulation since the principle of spreading (applied to a narrow band signal once) reduces its signal strength significantly [Ref.13].

The Naval Postgraduate School (NPS) has developed a satellite communications project that will investigate some of the operational characteristics of a spread spectrum communications link. This project, entitled "Petite Amateur Navy Satellite" (PANSAT), is proposed to employ a binary phase-shift keying communications package which will aid in developing insight into the development, successful delivery, operation, and management of an operational satellite communications system. As a major part of its mission it will provide a small operational test platform for a spread spectrum communications package. The project is scheduled for launch late in 1995 and will be fully operational by 1996.

This thesis examines a hardware solution for the development of a binary phase-shift keying (BPSK), direct sequence, spread spectrum modem to be implemented as one of the main communications channels to be used by PANSAT. The design developed in this thesis proposes a preliminary hardware design. The design described here is the first compact, operational prototype of a BPSK spread spectrum modem developed for the PANSAT project and will eventually be refined into a viable small satellite communications link.

II. MODEM DESIGN AND OPERATION

A. SYSTEM OVERVIEW

1. Modulation

The modulation section of the modem design consists mainly of three significant functional blocks. These are the division chain, the function generator and the pseudo-random noise (PN) generator. Each of these blocks takes a specified input and creates a waveform used in the generation of the BPSK spread spectrum signal. The modulator functional block is shown below as Figure 2.1 and is also shown in somewhat greater detail in Appendix A as Figure A.1.
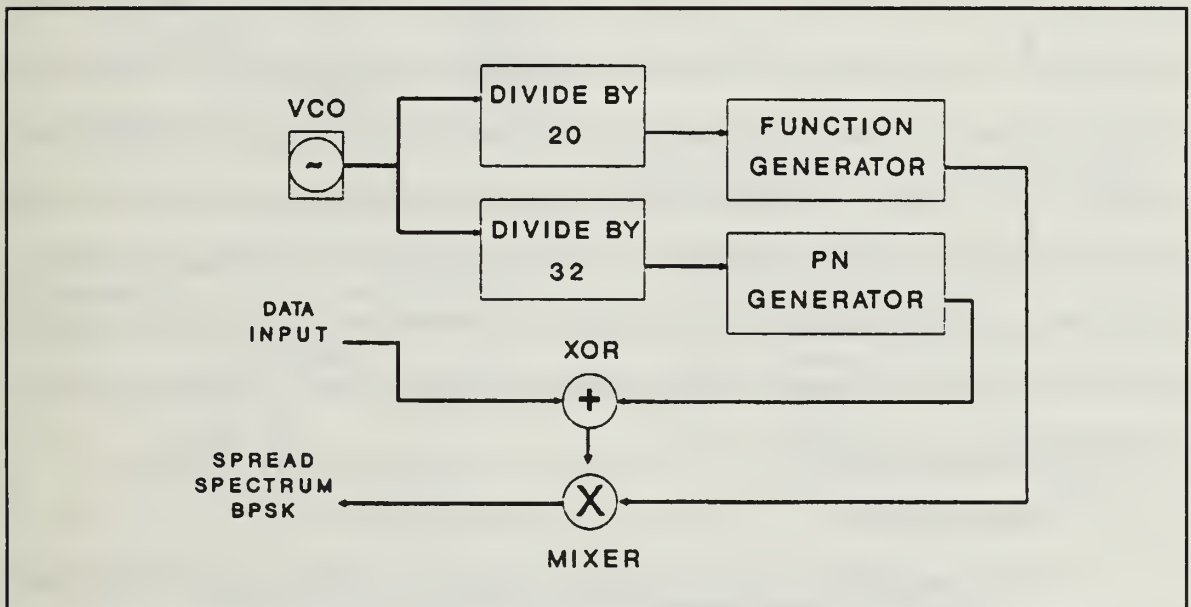
Figure 2.1: Modulator functional block diagram.

In the case of the division chain, the input comes from the crystal oscillator in a standard CMOS inverter configuration. In this design the oscillator acts as the master clock. Two reduced frequency waveforms are produced from

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the master clock providing the inputs to the remaining functional blocks. The outputs of the division chain are even multiple divisions of the crystal oscillator and are square-waves for reasons that will become clear as the operation of the circuit is discussed later in the chapter.

The function generator receives the higher frequency signal of the two square-wave outputs from the division chain. By the use of comparators, operational amplifiers and a precision sine-wave generator, the function generator outputs a sinusoidal carrier used in an intermediate frequency (IF) application. In the present stage of development for this design it acts as the carrier frequency. Up-conversion to the final radio frequency (RF) is a matter for further development implemented in the final PANSAT modem design. This thesis explores the potential for an experimental design in the implementation of a spread spectrum modem and investigates waveforms, relative signal strengths and acquisition and tracking control for the preliminary design using an IF loop-back form for testing the design. Hence, the development of the system is carried out through the IF stage. As more expensive precision components are used in the future, the design will be modified but, its functionality will remain the same. Thus, this thesis provides proof of concept for the modem design. Additionally, the final design must operate with significantly lower power consumption since power is limited in PANSAT.

2. Demodulation

The demodulation functional block diagram is clearly more complicated than that of the modulator. However, upon review, it demonstrates some of the elegance of as well as the complications involved in the development of a spread spectrum communications design. The functional block diagram itself consists of a division chain, PN generator and function generator. These have identical characteristics to those discussed previously in the modulation section. In

addition to these sections the demodulation process also requires a PN delay section, filtering and level detection, oscillator feedback control and output signal conditioning sections. The demodulator functional block diagram is shown in Figure 2.2 as well as in Appendix A as Figure A.2.

As mentioned above, the PN generator, division chain, and function generator sections are the same as those in the modulator and consequently, their outputs are identical to those employed by the modulator.
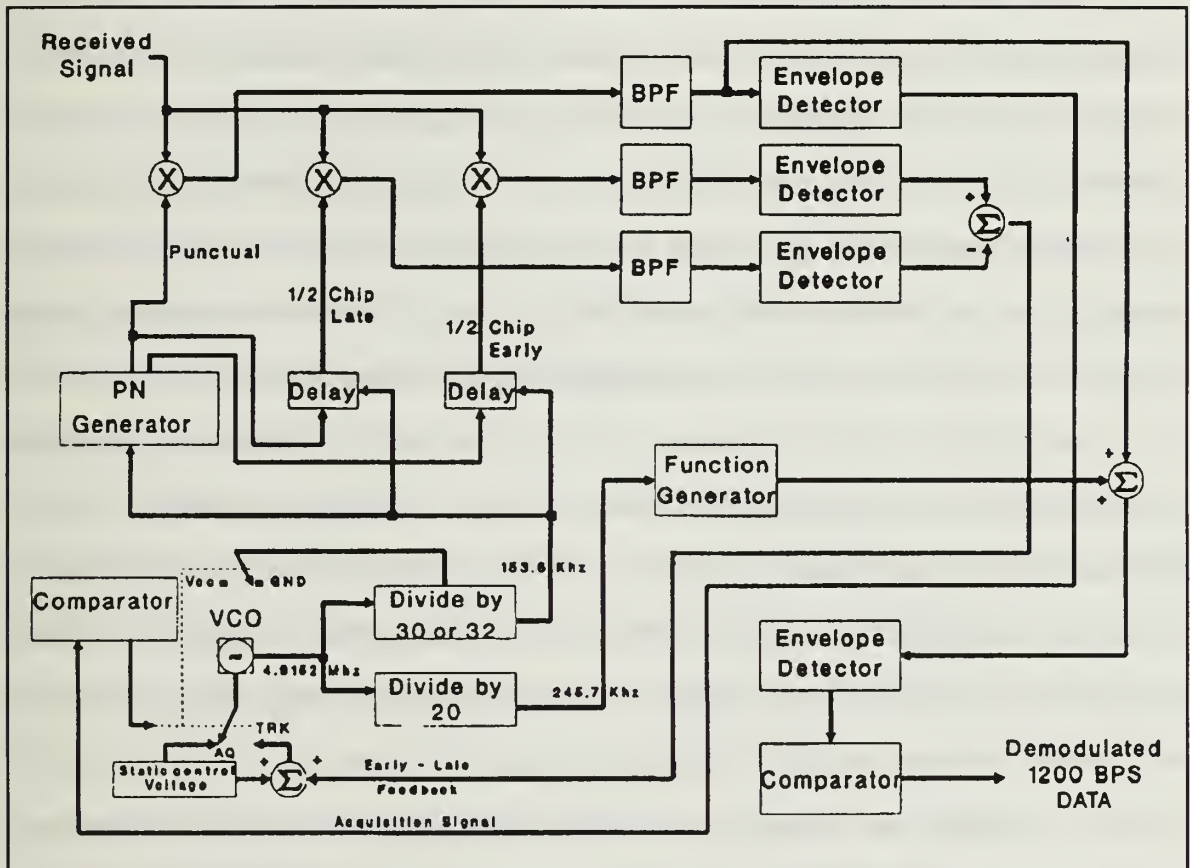
Figure 2.2: Demodulator functional block diagram.

The PN delay section provides the early and late PN sequences required for tracking the incoming signal. The phase relationship between the PN sequence used in modulation to spread the signal, and the PN sequence of the punctual

channel of the demodulator must be controlled in order to ensure that demodulation occurs [Ref.1:p.154].

During the acquisition phase of operation, the PN generator in the demodulator is driven at a higher clock rate (163.84 kHz) and the incoming signal is correlated with the output of the punctual PN sequence section. This point needs to be fully understood in order to appreciate the operation of the demodulator.

Acquisition time is critical in a system that employs spread spectrum techniques since data that passes without being correlated is obviously lost. Additionally, if the signal is lost, regaining acquisition as quickly as possible minimizes the overall data loss. This design uses a digital programmable divider to provide the appropriate frequency clock to the PN generators. By digitally changing the division factor (in the demodulator only) from a low value to a high value at the instant correlation occurs, the acquisition time is reduced drastically. In the perspective of the information bit rate, this design achieves a maximum acquisition time of 12 milliseconds. This corresponds to approximately 14.7 data bits and reflects the maximum number of bits lost from the commencement of acquiring the signal. However, it may be adjusted further to achieve a faster acquisition time. This is accomplished by changing the wiring connection at the programmable inputs to the divider and is discussed later.

Another key element of demodulation that occurs at the instant of acquisition is the shift of control voltage to the VCO. The VCO is shifted from static to dynamic feedback control utilizing the same punctual acquisition signal used to implement the change in the division of the PN clock. Dynamic feedback control is employed to control the frequency of the VCO in order to correct for potential drift of the transmitted PN sequence. Any significant drift would clearly degrade the ability of the demodulator to correlate continuously and prevent the

demodulator from providing a reliable communications link. These changes in PN clock frequency and VCO control correspond to the change from an acquisition mode of operation to that of a tracking mode of operation and vice versa.

While in the tracking mode of operation, the two parallel channels of early and late correlation provide a summed voltage feedback to the VCO via their respective band-pass filters, corresponding signal level detectors, and an inverting and summing set of amplifiers. Utilizing this feedback voltage the frequency of the VCO tracks the frequency of the incoming signal and maintains an in-phase or coherent phase state for the demodulator. The signal, as it appears from the output of the punctual channel during tracking, is no longer spread spectrum since the PN sequence has been stripped from the carrier by a mixing operation with the output of the punctual PN generator. This in turn, implies that the signal output from the mixer is a BPSK modulated wave whose frequency is that of the IF frequency. All phase shifts that now occur are merely the result of the transmitted data.

While the master clock is maintained in track mode, coherent demodulation of the data takes place. By nature of the fact that the function generator (producing the sinusoidal IF carrier) is also controlled by the master clock, the phase relationship of the carrier waveform is also maintained constant. While in the track mode of operation, the output of the punctual channel is combined with the output of the function generator to produce a signal representative of the original transmitted data. An AD534JD is configured to simply add the signals. Its output signal is passed through a conditioning circuit to produce the recovered data at voltages representative of TTL data (0 and +5 volts) and is discussed later in this chapter.

B. DIVISION CHAIN

1. Modulator

The clocking and function generator waveforms required for the modulator consist of two square-waves. These are generated by programmable division of the 4.9152 MHz crystal oscillator which acts as a master clock. Since the same timing sequences are required for both modulation and demodulation, the configuration for the division chain hardware is identical except during pre-acquisition mode as mentioned next in the demodulator discussion. In the modulator, the PN sequence square-wave (153.6 kHz) and the square-wave used in the function generator section (245.7 kHz) are whole multiple, cumulative divisions of the master clock by factors of 32 and 20 respectively. To achieve these division multiples, two four-bit, synchronous, binary up/down counters (54193) are used in parallel channels in conjunction with a J-K flip/flop (74112 for the PN sequence clock) and two J-$\overline{\text{K}}$ flip/flops (74109 for the function generator). The flip/flops in each case contribute a factor of two to the overall division of signals at their respective inputs. For this reason the counter division multiple for the PN clock is set to 16. Since two flip/flops are utilized in the derivation of the function generator square-wave, their contribution to the overall division factor of the master clock is a factor of four. Consequently, the 54193 division multiple in the function generator division chain is set to five.

The output of each terminal flip/flop is by design the square-wave representation of the desired clock at the desired frequency. The circuit diagram for the modulator division chain is shown in Figure B.1 and is located in Appendix B. A representative set of waveforms for the crystal oscillator and the 153.6 kHz and 245.7 kHz square-waves appear as Figures 2.3 and 2.4 later in this chapter.

The 54193 is a four-bit, programmable, binary counter which when driven by the master clock outputs a reduced frequency pulse train. The division value is set by its four data input pins. These programmable counters are employed to aid in the future design flexibility for adaptations to the division chain. This is in anticipation of their use with a higher frequency (and more precise) voltage-controlled oscillator (VCO) serving as the master clock. This also supports the possibility of digital feedback control of the VCO. Additional counters employed as dividers can easily be arranged in series with the existing design when needed for adaptation to a final space ready modem adding greater flexibility to the division chain.

2. Demodulator

As mentioned above, the hardware configuration of the demodulator division chain differs only slightly from that of the modulator. The PN generator clock is designed to operate in two distinct modes (acquisition and track) and, depending on the mode, outputs one of two clock frequencies. While in the acquisition mode, the programmable counter is set to divide by 15 vice 16 creating a total division (including the flip/flop) of 30 vice 32. The resulting clock drives the PN generator in the acquisition mode at a frequency of 163.84 kHz vice 153.6 kHz. This creates a rapid convergence of the PN sequence to its relative synchronized correlation with the PN sequence of the received signal. It also serves as a small demonstration of the overall design flexibility that may be exploited if a micro-controller is used for digital frequency control in future designs.

Once the PN sequence is at the appropriate position relative to that of the incoming signal, the correlation signal from the punctual channel triggers an analog switch (PWI SW06) to change the division performed by the programmable divider from 15 to a value of 16. Subsequent refinement of the

frequency is then assumed by the VCO feedback circuitry. The circuit diagram for the demodulator division chain is located in Appendix B and is Figure B.5.

C. PN GENERATOR

1. General

The pseudo-random noise (PN) generator used in both the modulation and demodulation sections of the BPSK communications package is driven by the clock generated from the crystal oscillator via the division chain as described in section 2.B. The crystal frequency was chosen arbitrarily to be a 4.9152 MHz fundamental frequency from readily available components. This frequency, when divided by a factor of 32, creates the 153.6 kHz clock frequency which then corresponds to the chip rate for the system.

For compliance with Federal Communications Commission (FCC) rules governing the implementation of SS communications systems in the amateur radio frequency bands, a seven-bit sequence (one of three allowed) is used on PANSAT [Ref.6:p.21-14]. BY design, each data bit will contain 127 chips (an entire sequence) of the PN sequence. A final space-ready design of PANSAT (supporting a data rate of 1200 bits per second) must have a clock frequency and corresponding chip rate of 152.4 kHz. This arises from the FCC constraint of containing an entire epoch (127 chips) of the spreading PN sequence within exactly one data bit of the digital information to be transmitted.

Since the design developed in this thesis is intended to show proof of concept for the development of the SS modem, the modified chip rate was chosen so that it might closely simulate that of the final design while forgoing the expense of a customized oscillator. The fundamental operation of the system will not change appreciably when altered to the final chip rate of 152.4 kHz.

2. Technical

a. Modulation PN Sequence Generation

For the hardware design of the modem the chip rate is established through the programmable divider and a J-K flip/flop (refer to circuit diagram B.2 in Appendix B). The oscillator output is pictured in Figure 2.3. Use of a flip/flop in this application is essential to create the symmetric square-clock waveforms. The square-waves are necessary to establish both the early and late tracking PN sequence relationships for synchronization feedback used in the delay-lock loop. Additionally, a synchronous square-wave is needed in the generation of the sinusoidal carrier for this design. In the modulation section a square-wave clock is not required for generation of the PN sequence since no companion PN sequences (either early or late) are used. The identical configuration for the clock generation is employed nonetheless in both the modulation and demodulation sections in order to provide continuity of design. Since synchronization PN sequences are clearly neither generated nor used in the modulator, a final design containing both a modulator and demodulator as a unit may likely share the same PN generator but only for conservation of limited spacecraft power. For this additional reason, square clock waveforms are used throughout this design and can be implemented in just this way for the final space ready design.

The division chain hardware in the modulator is not as complex as that of the demodulator since synchronization and tracking are accomplished only in the demodulator. Each of these division chain implementations was discussed in detail in section 2.B of this chapter. Only two key clocking waveforms are generated in the modulation section. These are the PN clock (153.6 kHz) and the square-wave used in sinusoidal carrier generation (245.7 kHz).

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The PN generator itself consists of an eight-bit shift register (74LS164), two exclusive-or (XOR) gates (7486) and a synchronous binary counter (74161). The elementary design was taken from Reference 6, p. 21-12, although many variations are available from other literature sources. This design features simplicity as well as a desirable zeros-catching function preventing the shift register from becoming locked in an all-zeros state.
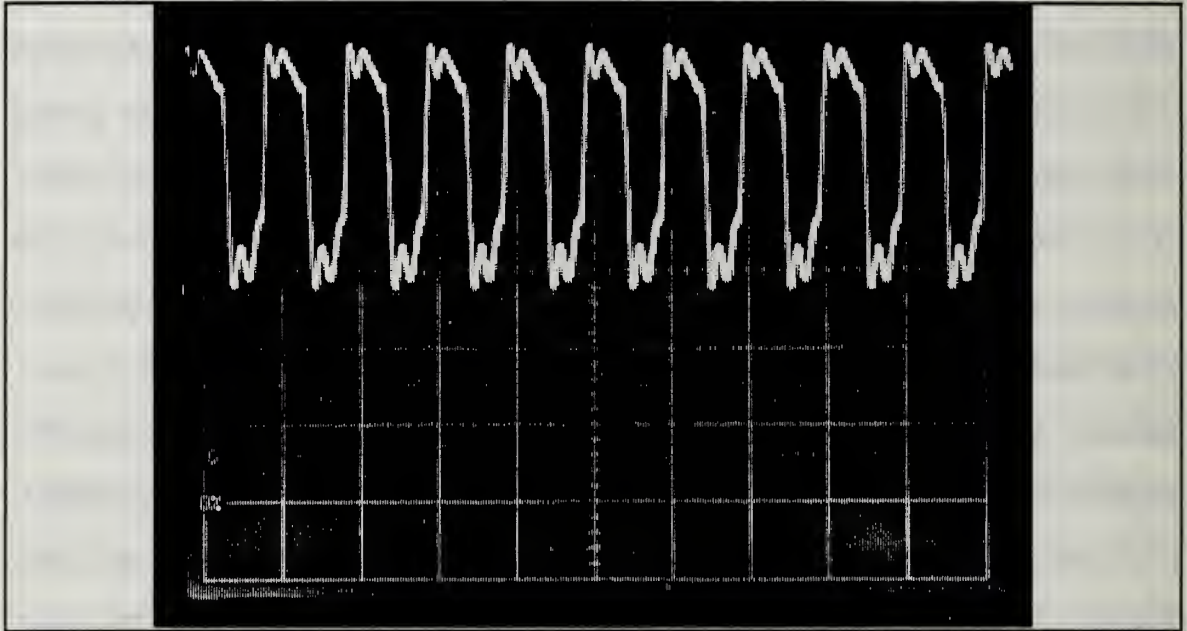
Figure 2.3: Crystal oscillator output.
Oscilloscope settings: X = 0.2 μsec/Div., Y = 2.0 v/Div. .

The design is modified to include a synchronous binary counter for the addition of a ones-catching capability since operation of the design without it is unreliable and occasionally locks the shift register in an all-ones state. An alternate ones-catching circuit utilizes an eight input NAND gate vice a counter. Implementation of ones-catching by a NAND gate was considered for this design and would work equally well. However, the synchronous binary counter was used to minimize the number of wiring connections.

The shift register itself creates the PN sequence through modulo-2 addition of the outputs of two stages of the shift register (refer to Figure B.2 in Appendix B). In this design the first and seventh stages of the shift register are modulo-2 added by way of an XOR gate (the eighth register is not used). The resultant logic level is fed back to the input of the first stage of the shift register via a second XOR gate on which the companion input terminal is tied to +5 volts ("high"). This second XOR acts as an invertor but functions as the zeros-catching logic gate. Without this second XOR gate, initial power-up of the PN generator will leave all values in the shift register as well as the input to the first stage register at 0 volts ("low"). They will remain low as feedback cannot reach a high logic level without artificially loading a high level into one of the first seven stages. The clock sequences for PN generation as well as the square-wave used for sinusoidal carrier generation are shown in Figure 2.4.

Also essential to the reliable operation of the PN generator is the ones-catching property of the synchronous binary counter. Simply stated, the 74161 is driven at the chip rate by connecting its clock input to the same clock that drives the shift register. The PN sequence output of the shift register is connected to the clear pin on the counter which is active-low. Every time a zero is produced during PN sequence generation the counter is cleared. The maximum number of consecutive ones in the sequence is seven. This prevents the counter from reaching a count of 16 while monitoring the activity of the shift register during the generation of the PN sequence. If all stages of the shift register simultaneously reach a high logic level, the binary counter will continue to count without being asynchronously cleared since the PN sequence is locked in an all-ones state by the zeros-catching XOR gate. The ripple carry output of the counter is tied to one input terminal of an XOR gate on which the companion input terminal is tied high. The XOR output is connected to the clear pin of the

shift register. In this way, the detection of an all-ones state will be corrected by an asynchronous clear of the shift register.
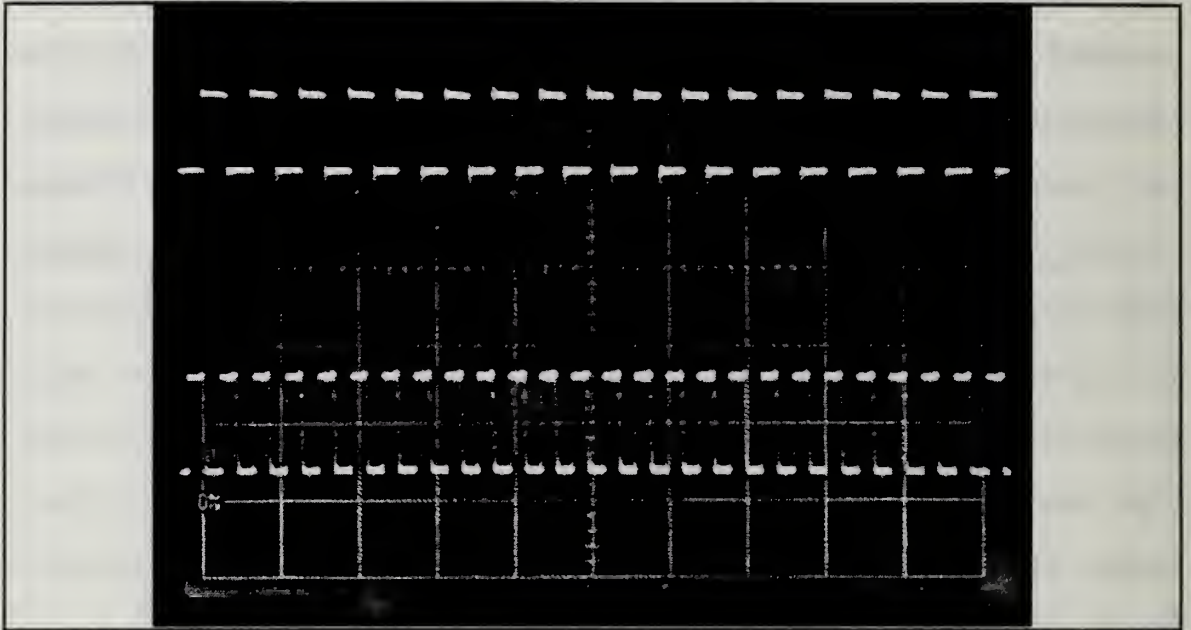
Figure 2.4:
Top: PN generator clock.
Bottom: Function generator clock.
Oscilloscope settings: X = 10 μsec/DIV., Y = 5 v/Div. .

The XOR gates employed in the PN generator for zeros- and ones-catching merely act as inverters. The XOR gates are used here vice inverters simply because of the availability of the unused XOR gates on the 7486 chip used for modulo-2 addition in the PN generator section.

Once the shift register is cleared, the binary counter is also cleared allowing the sequence to resume generating normally. The counter itself is actually cleared after a count of seven from the resumption of normal PN sequence generation since the clear pin on the counter is tied directly to the output of the zeros-catching XOR gate. The seven shifts are required to create the necessary active-low condition appear at the clear pin of the counter. Thus,

the counter is still prevented from reaching a count of 16 and normal PN generation continues.
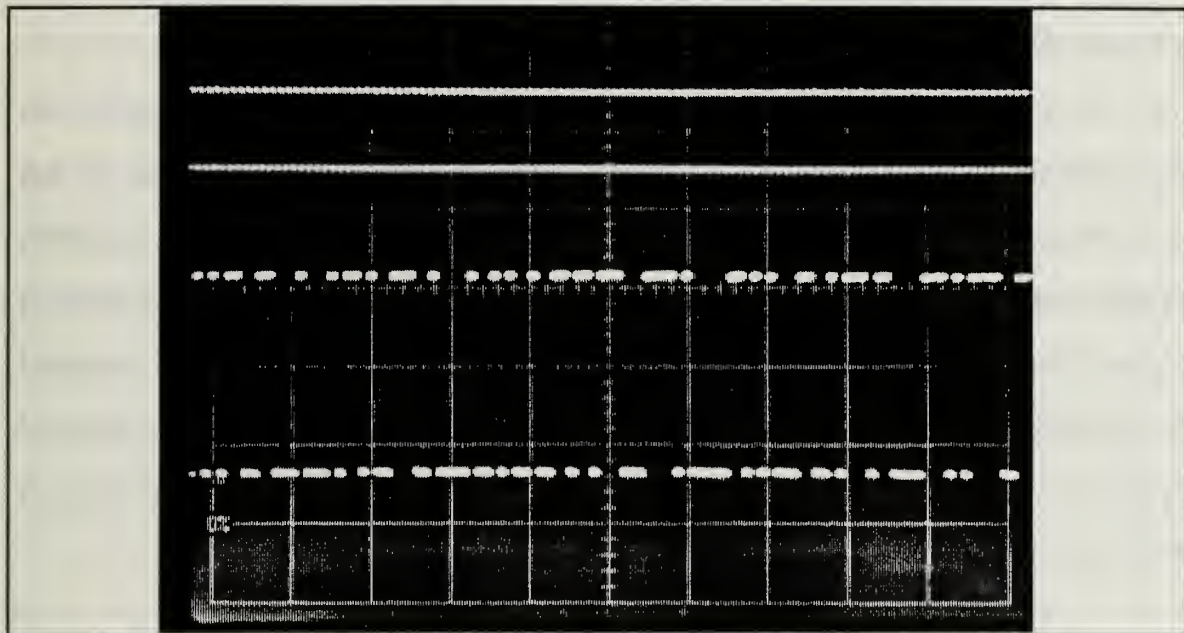
Figure 2.5:
Top: PN generator clock (153.6 kHz), 2 v/Div. .
Bottom: PN sequence used for spreading, 5 v/Div. .

The resultant PN sequence, assuming normal uninterrupted operation, is a maximal length sequence consisting of series of high and low logic levels (ones and zeros) in pseudo-random order. This binary sequence is repeated every 127 clock cycles and each sequential pattern is identical. The periodicity of the sequence results from the relationship in Equation (2.1) which relates the number of stages in the shift register employed (m) to the length of the sequence (L), up to the point of repetition [Ref. 1:p.58].

$$L = 2^m - 1 \qquad\qquad (2.1)$$

A representative sample of the actual maximal length PN sequence used in both the modulation and demodulation sections is shown in Figure 2.5

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along with the 153.6 kHz clock. In actuality there are only approximately 100 of the 127 chips represented in Figure 2.5. This is due to the triggering of the waveform on the oscilloscope and the settings used to produce an illustrative photograph of the PN sequence.

Three identically configured PN sequences are employed in the demodulation section and are used in the acquisition and tracking of the incoming signal. VCO feedback control is required in order to maintain synchronization and enable the demodulator to continuously track the incoming signal. For this reason, two additional PN sequences of the identical maximal length (127 chips) are generated at a 1/2 chip timing offset relative to the PN sequence used to acquire and demodulate the received signal. The demodulation PN sequences are discussed next.

b. Demodulation PN Sequence Generation

As will become evident in the following sections, three PN sequences (identical to that of the modulator) are required for acquisition, tracking, and consequently demodulation of the received spread spectrum signal. These sequences are termed "punctual", "early" and "late."

Generation of the punctual sequence in the demodulator is identical to that of the modulator described earlier and the hardware remains the same. The early and late PN sequences are generated by delaying the outputs from the sixth and seventh stages of the shift register by 1/2 chip respectively. For the early sequence, the output of the sixth stage of the shift register is sent to an inverter for buffering. This inverted sequence is sent to a second inverter. These inversions produce two PN sequences that remain one chip early but are logical compliments of each other. The complimentary sequences are then tied to the J and K inputs of a 74112 J-K flip/flop to produce the delay.

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The same clock used for the shift register is connected to the 74112. The 74112 utilizes a falling clock transition and, in the configuration shown in Appendix B, acts as a single bit shift register. Since the J and K inputs are always compliments of each other they are shifted to their respective Q and $\overline{Q}$ outputs when the flip/flop is clocked. Since the clock transitions for the shift register and the flip-flop posses opposite transition states (rising for 74LS164 and falling for 74112), the arrival of the complimentary PN sequences at the input of the 74112 is guaranteed to be 1/2 chip prior to the falling edge of its clock. The resultant output from the 74112 is a PN sequence identical to that of the punctual one but whose timing appears advanced by 1/2 chip relative to the punctual sequence.
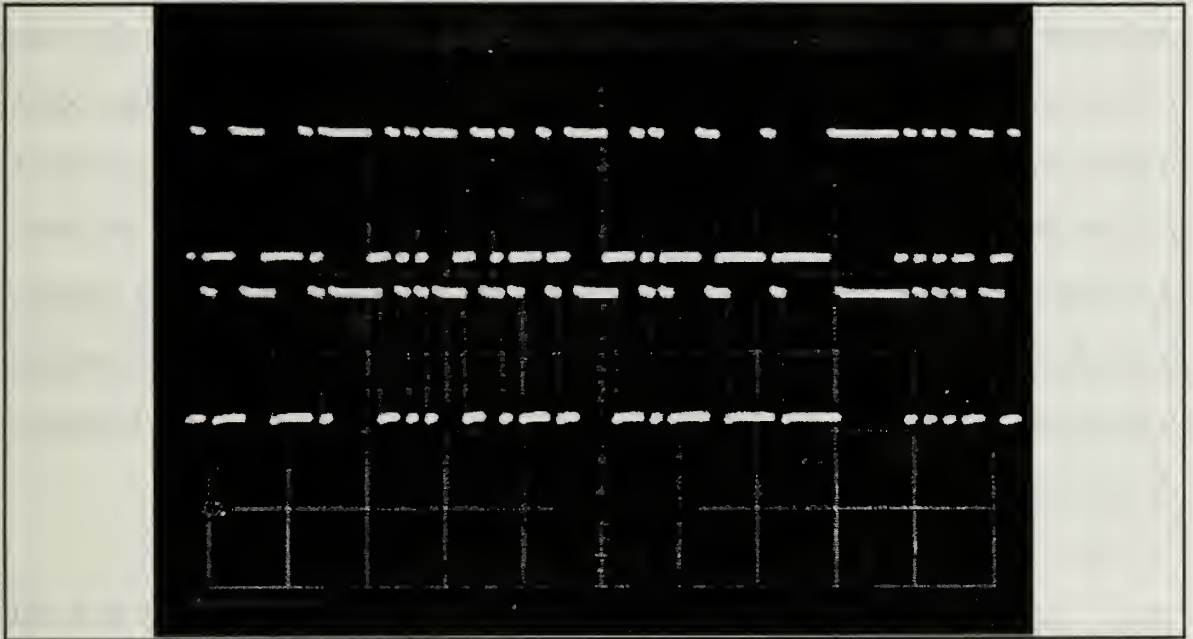
Figure 2.6:
Top: Early PN sequence.
Bottom: Late PN sequence.
Note: One chip differential.

The late PN sequence is created in the same fashion differing only in that the parent sequence taken from the shift register is the punctual sequence itself and results in a PN sequence whose timing is delayed by 1/2 chip relative to

the punctual sequence. Consequently, the same hardware discussion applies as well. The relative positions of the early and late sequences are shown in Figure 2.6 and the circuit diagram for the demodulation PN generator appears as Figure B.5 in Appendix B.

D. FUNCTION GENERATOR

1. General

The function generator creates the sinusoidal carrier used in the transmission of the spread spectrum signal at the IF frequency. The generation of a sinusoidal carrier can be accomplished in many different ways but the particular solution depicted in this design is the most practical one given its minimal cost. Although minimized cost is not a requirement for a prototype design, in this case readily available components are used due to the intent of this design being mainly proof of concept. All concepts used in this as well as other sections of the modem design are fully adaptable when more sophisticated components are used. Additionally, the basic functionality of the design will not appreciably change. Since both the modulation and demodulation sections create their sinusoidal waveforms in the same manner, the technical description as well as the hardware design applies to both.

2. Technical

A circuit diagram for the function generator is shown in Figure B.3 and is located in Appendix B. The function generator section receives a square-wave at the frequency of 245.7 kHz from the division chain. The square-wave is converted from TTL voltages and their associated low driving currents to the appropriate values required by the analog components used in the generation of the sinusoid. This is accomplished by interfacing the output of the division chain through a comparator.

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The output of the division chain is fed to the negative input pin on a voltage comparator (LM311P) which is configured to produce an output to supply a ground referenced load [Ref.7:p.2-54]. Two 1KΩ potentiometers are used to establish the positive and negative peak values of the resultant square-wave at +2.5 and -2.5 volts. These are derived from the +15 and -15 volt power supplies used throughout the analog portion of this design.
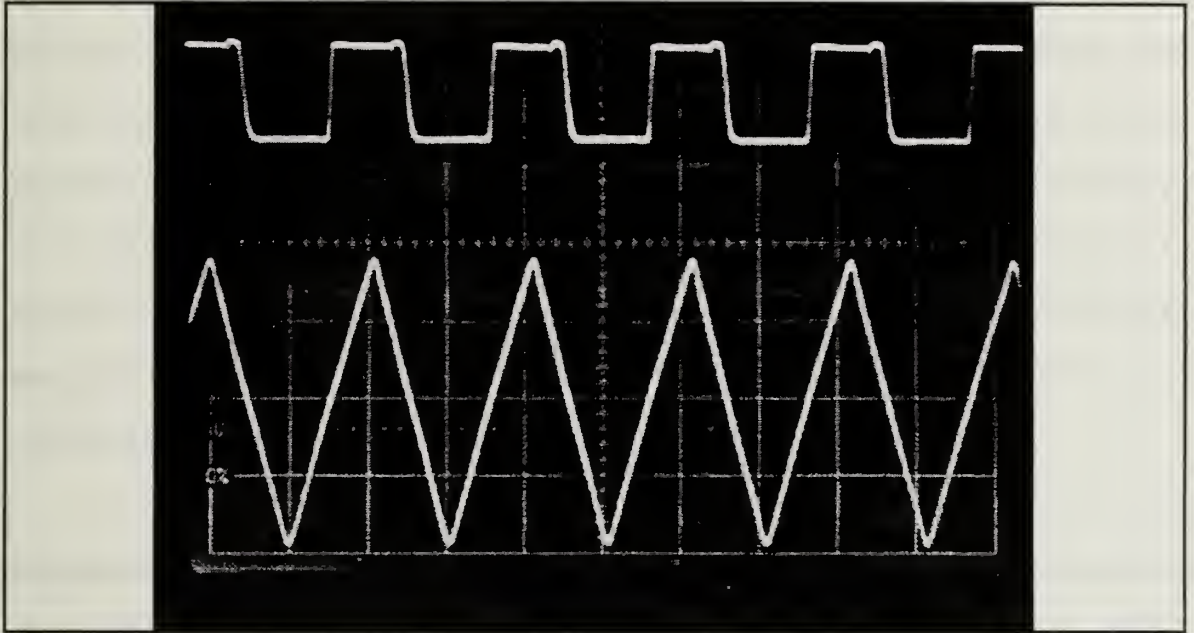
Figure 2.7:
Top: 245.7 kHz Square wave; LM311P output.
Bottom: Triangle wave output of LM318N integrator.
Oscilloscope setting: X = 2 μs/Div. , Y = 5 v/Div. .

The threshold voltage is clearly a positive value since the input square wave is a TTL signal. The threshold voltage is established through the center tap of a 10KΩ potentiometer connected to the +15 volt supply and is adjusted to ensure a balanced square-wave output. The voltage value for the reference voltage threshold in this design is measured from the completed circuit board at pin 2 of the LM311P. This voltage is +2.50 volts as expected given a consistent standard TTL input.

The use of both 0.1µf ceramic and 1.0µf tantalum capacitors as power supply bypass capacitors is absolutely essential to produce a noise free output from the LM318N [Ref. 8:p.42]. In addition, a 30pf capacitor is used between pins 1 and 8 on the LM318N to stabilize the output waveform. The design without the addition of the previously mentioned capacitors does not function.
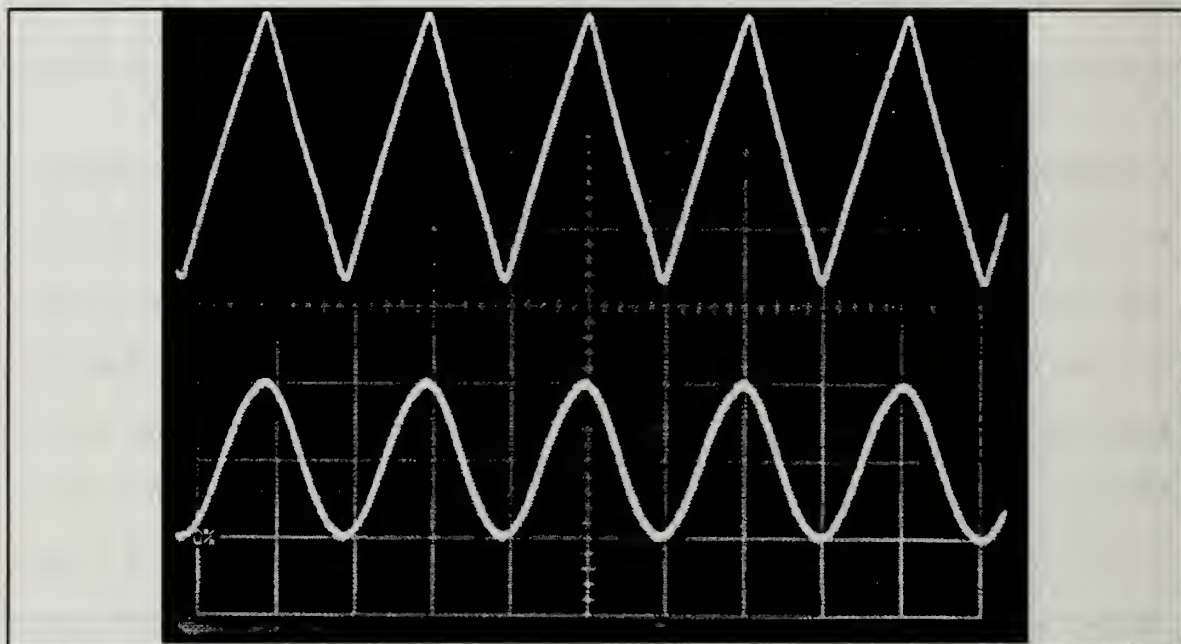
Figure 2.8a:
Top: Triangle wave following voltage divider.
Bottom: 245.7 kHz Sinusoidal output.
Oscilloscope settings: X = 2 µs/Div. , Y = 1 v/Div..

For the transition from a square-wave to a suitable waveform for sinusoidal generation, the 245.7 kHz square-wave is sent from pin 1 of the LM311P to the inverting input pin of an operational amplifier (LM318N) which is configured as an integrating amplifier [Ref. 5:pp.164 & 268]. The capacitance value used in the feedback loop is 68pf and is in parallel with a 240KΩ resistor. Supply voltages V+ and V- are taken directly from the +15 and -15 volt power supplies. The output of the LM311P as well as the output of the integrating LM318N is shown in Figure 2.7.

The resulting triangle wave is connected to pin 1 of a universal trigonometric function generator (AD639AD) via a resistance voltage divider. The voltage divider serves to limit the input voltage to the AD639AD to a designed maximum peak voltage of 1.8 volts and thereby minimizes distortion in the generated sine wave. These resistance values (R19 and R20) are fixed as shown in Figure B.3 located in Appendix B. Since the amplitude of the triangle wave is dictated by the amplification set by the integrator (component U13 in Figure B.3), the use of a potentiometer for voltage reduction is not required. Consequently, for adaptations of future designs using this configuration, replacement of the potentiometers in the comparator circuit preceding the function generator section may require only a slight adjustment. In addition, potentiometers are not expected to be utilized in a space flight model due to the potential for drift when exposed to vibration. In any case, the peak input voltage of 1.8 volts to the AD639AD is easily realizable utilizing fixed resistors.

The AD639AD is configured for sine-wave output [Ref. 5:p. 162]. A representative sample of the sinusoidal output of the function generator section is depicted along with its input triangle wave in Figure 2.8a. The sinusoidal waveform undergoes no additional amplification prior to the mixing operation employed to produce the spread spectrum signal in this design. There is however room for amplification since the maximum input voltages for the mixer (discussed in the next section) are not approached here. Further amplification is expected to be accomplished in a final design where up-conversion will be required and attenuation induced by power conserving, passive elements will be encountered.

E. MIXERS

1. General

The BPSK modulated signal output of the mixer in the modulation section is the result of the combination of the PN encoded data stream with the sinusoidal carrier. Mixing operations for the BPSK spread spectrum modem in this design, or in general where digital SS BPSK is used, occur in two places. The 1200 bps data stream is modulo-2 added to the PN sequence in the modulation section creating the PN encoded data stream. An XOR gate is used for this process and since the inputs to the XOR gate are TTL voltages with a bipolar characteristic, the function performed by the XOR is essentially a mixing operation. This fact may seem trivial but creates an important dual as concerns the treatment of the signal in modulation and its subsequent demodulation.

The TTL voltages are converted to plus and minus voltages for interfacing with the analog components in this design. The mixing of the data, PN sequence and sinusoidal carrier can be accomplished in any order while still producing the same BPSK spread spectrum result. As will be discussed in the demodulator discussion, the PN sequence is removed from the spread signal first.

2. Technical

a. Modulation

The mixers employed for modulation consist of an XOR gate and an internally trimmed, precision IC multiplier (AD534JD). The AD534JD is also commonly known as an analog voltage multiplier.

The inputs to the XOR gate are the TTL data stream (at 1200 bps) and the PN sequence generated by the PN generator section of the modulator. The output of the XOR gate can be thought of as essentially a bi-phase shifted PN sequence. Considering the length of the sequence (127 chips) as one period, each data transition (which contains 127 chips) causes the PN sequence to invert.

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The PN sequence phase relationship is then similar in fashion to that of a bi-phase shifted sinusoid since the PN sequence is also a periodic waveform.

The design in this case only closely approximates the chip rate of the final design and instead of containing exactly one entire PN sequence (127 chips) within one data bit there are only 126.0078125 chips per bit. This of course was discussed in the PN generator section and will need to be altered to comply with FCC rules. The fundamental operation of this BPSK spread spectrum design is independent of the number of chips per bit and any alterations to meet this specification for use in PANSAT will have no effect on the performance of the design.

The maximum periodicity by which the PN sequence chips will be inverted is the reciprocal of the data rate (or 833.33 μsec). The associated phase change of the PN encoded sequence occurs in intervals of less than or equal to the period of one data bit. An alternating data sequence (square-wave) creates the maximum periodicity of inversions to the PN sequence. For testing purposes a 600 Hz TTL square-wave is used to simulate the 1200 bps data stream.

The resulting PN encoded data stream is interfaced with the AD534JD by means of a voltage comparator (LM311P) which is configured for an output supply to a ground referenced load (a complete discussion of this comparator configuration is given earlier in part D of this chapter). The reference potentiometer supplies a voltage of +2.50 volts to the minus input of the LM311P. The V+ and V- potentiometers are set to supply +10.0 and -10.0 volts. Each of the potentiometers can clearly be replaced by a set of precision resistance voltage dividers. The resultant output is a balanced PN encoded sequence with bipolar voltages of +10 and -10 volts. This signal is connected directly to pin 6 of the AD534JD which corresponds to its Y1 input. The sinusoidal carrier from the function generator section is also connected directly to the AD534JD on pin 1

which corresponds to the X1 input. The AD534JD accomplishes multiplication according to the formula labeled Equation 2.2 [Ref.9].

$$\frac{(X1 - X2)(Y1 - Y2)}{10} + Z2 \qquad (2.2)$$

The wiring configuration for the mixers shown in Appendix B as Figure B.3 and is taken from Reference 9. This reflects a standard multiplication configuration and functions equally well as a mixer. This component can be easily replaced throughout the design by passive doubly-balanced mixers and will be required for this design eventually to minimize power consumption as well as accommodate a higher IF.

Figure 2.8b:
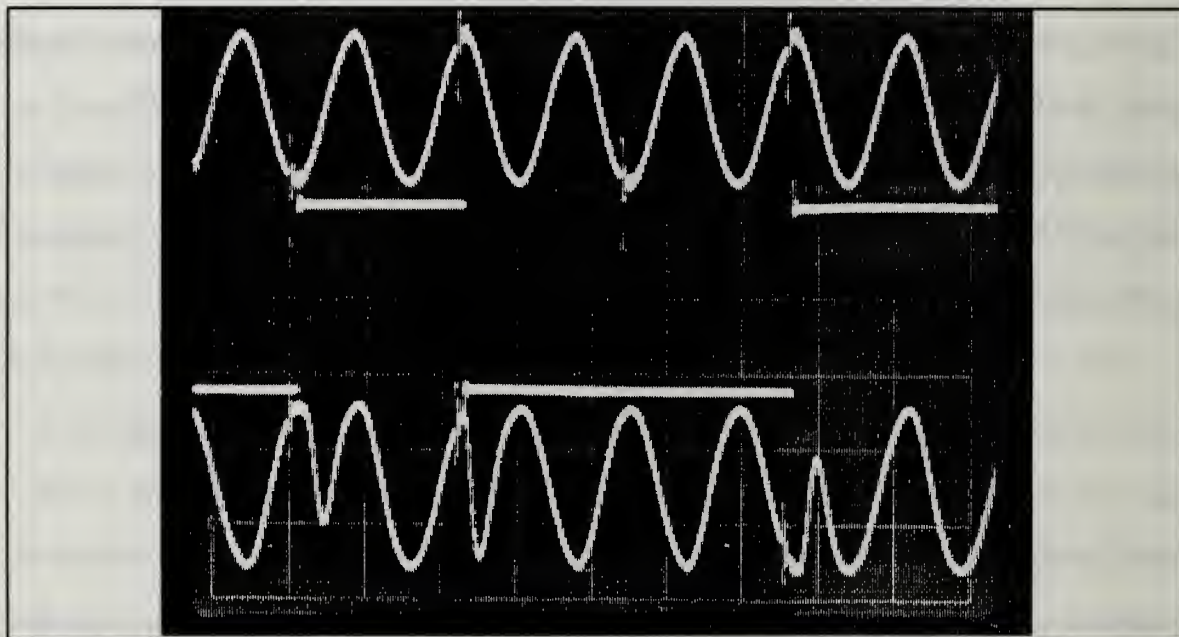**Top: Sinusoid from function generator section.**
Middle: PN encoded data output from comparator.
Bottom: Spread spectrum BPSK output at 245.7 kHz.

An SRA-8 doubly-balanced mixer was used early in this design but the AD534JD is favored here for adaptability to the overall breadboard design. The input and output waveforms of the AD534JD are shown as Figure 2.8b and are

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representative of approximately five chips of PN encoded data or 1/25th of one data bit at the proposed data rate of 1200 bits per second. From the oscilloscope trace it is clear that the output of the modulator is a BPSK signal with a pseudo-random phase change. The relationship between the unmodulated carrier, BPSK modulated carrier (1200 bps data modulation only), and spread spectrum BPSK modulation (PN encoded data modulation) is seen clearly upon examination of their respective frequency spectrum outputs.
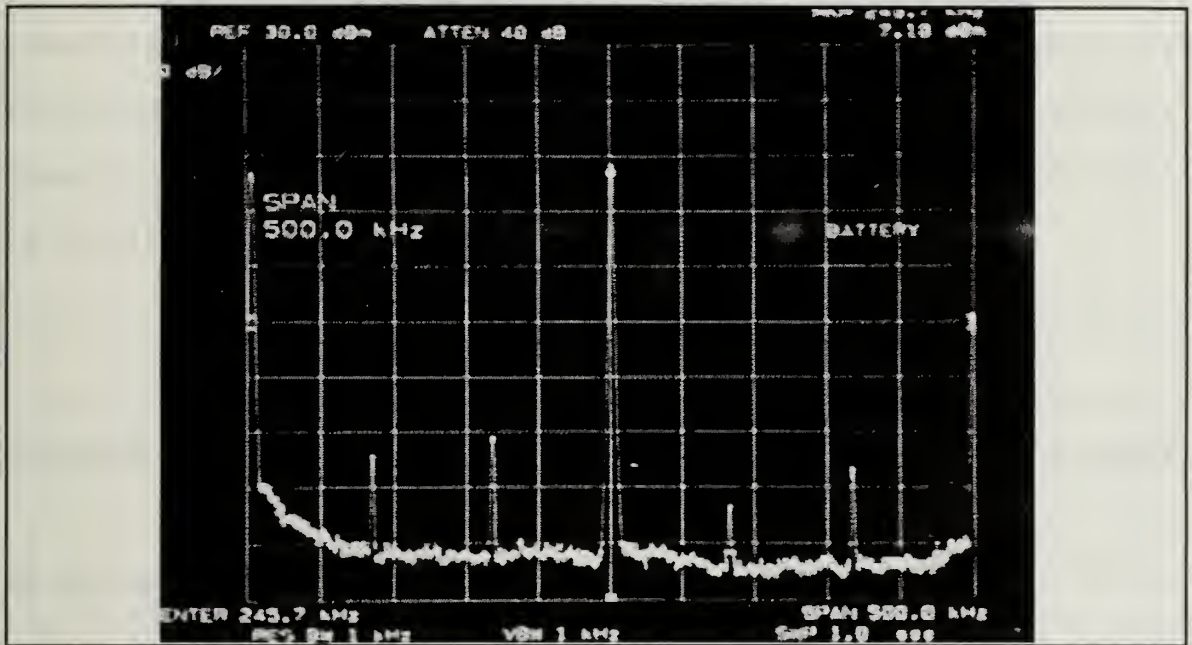
Figure 2.9a: Frequency spectrum for the sinusoidal carrier(unmodulated) taken from the output of the function generator section.

The frequency spectrum for the unmodulated carrier is taken directly from the output of the AD639 function generator. In the case of the two modulated waveforms, their spectral outputs are created by connecting the associated modulating square-waves to the Y1 input of the AD534JD and maintaining the 245.7 kHz carrier connected to the X1 input. The output is taken from the OUT and Z1 pins which are tied together. The AD534JD does not operate properly when the inputs X1 and Y1 are swapped and therefore Equation

2.2 only applies to the configuration shown in Appendix B for mixing with the sinusoidal carrier. The Z2 pin is grounded and therefore contributes nothing to the offset value depicted in Equation 2.2.
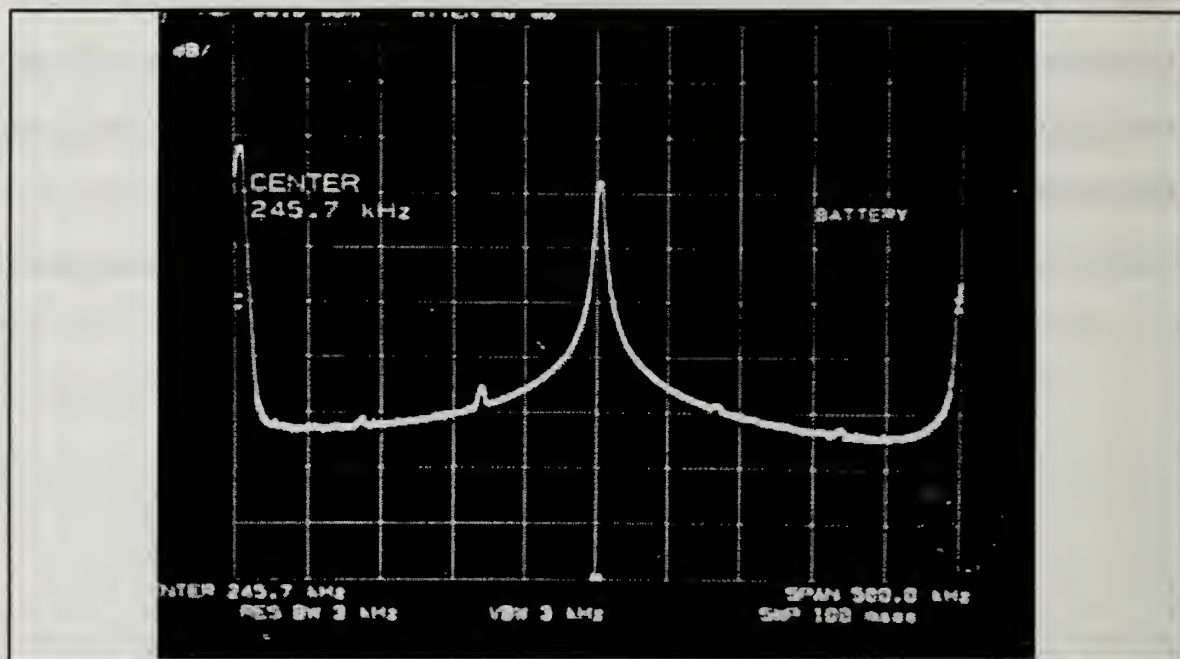
Figure 2.9b: Spectrum for 1200 bps BPSK modulated carrier. A square wave at 600 Hz is used as the data stream.

The Spectrum outputs are shown for each of these three cases as Figures 2.9a through 2.10b and are taken from a spectrum analyzer set to a bandwidth of 500 kHz and centered at the carrier frequency. The spectrum seen in Figure 2.9b as compared to that of the unmodulated carrier demonstrates that the bandwidth of the spectral main lobe and associated side lobes widens. The bandwidth of concern is that of the main lobe since it is the only portion of the spectrum transmitted in most BPSK modulation schemes. In fact, no significant gain results from the transmission of the side lobes since an overwhelming fraction of the spectral energy is contained within the main lobe [Ref. 6:pp.21-12,21-13]. This well known characteristic remains true in the application of this spread spectrum design.

The frequency spread of the BPSK spread spectrum signal is twice that of the chip rate. This is clear when the characteristics of the PN sequence encoded data stream are examined. Since the chip rate is several times greater than the data rate, the modulo-2 added sequence assumes the frequency characteristics of the PN sequence. Moreover, since the chip rate is 153.6 kHz the corresponding main lobe bandwidth is approximately twice this value or 307.2 kHz as seen in Figure 2.10b. The actual main lobe bandwidth, as determined from the spectrum analyzer, is somewhat difficult to measure exactly since the spectrum takes on a noise spectrum with a $(\sin(x)/x)^2$ characteristic as is depicted in Figure 2.10b [Ref. 1:p.16]. The main lobe bandwidth for this design is however consistently approximated from the spectrum analyzer output at a value of 310 kHz and is the IF bandwidth for the demodulator [Ref.4:p.50].
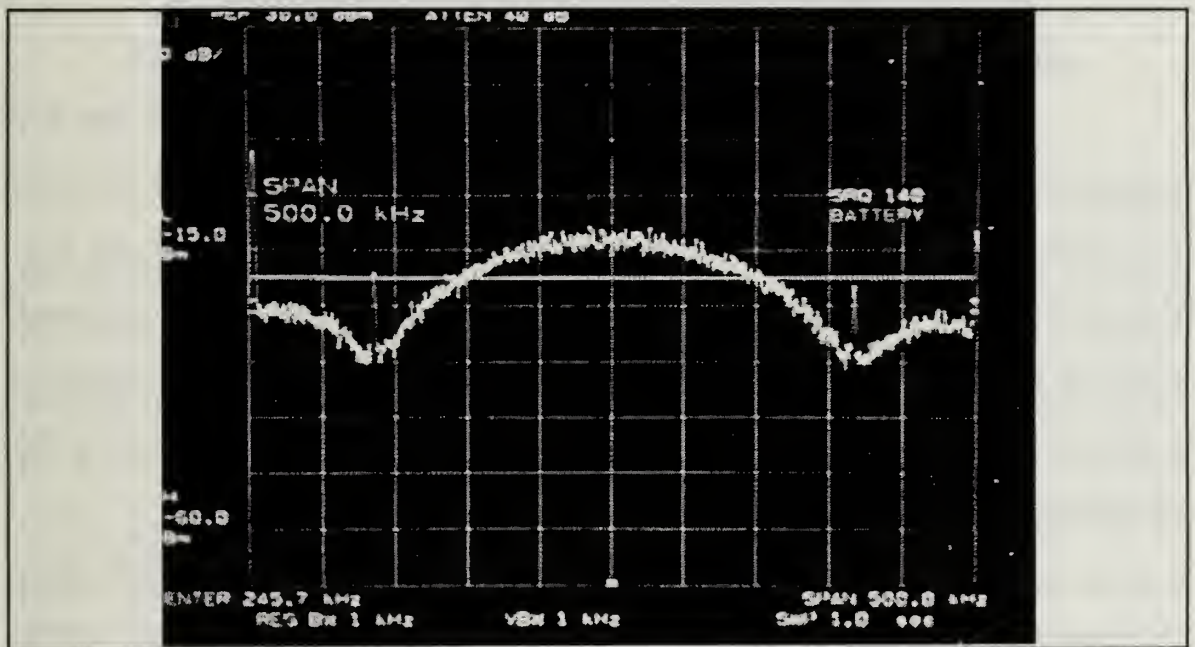

Figure 2.10a: Spectrum for the PN encoded BPSK (spread spectrum) modulation. The max. hold setting is enabled on the analyzer.

The spread spectrum signal is transmitted from the modulation section of the modem design in an IF loop-back testing configuration and is connected directly to the demodulation section. This provides for testing the proof of concept for this design as the majority of the complications associated with spread spectrum communications design arise from the inability to acquire and track the spread spectrum signal.

There is no output filtering conducted within the modulation section of this design and hence all spectral components are received by the demodulator in the IF loop-back channel. Output filtering at the modulator would have no significant effect on the performance of this design and it is expected that adaptations of the modem described here will employ wide band filtering of the transmitted signal at the appropriate RF frequencies centered at 437.25 MHz.

b.   *Demodulation*

The demodulation process reverses the order in which the PN sequence and the data are combined with the IF carrier. This is possible since the processes of mixing are order-independent as discussed earlier. Thus, the first thing to be removed from the incoming signal is the PN sequence. As discussed earlier in this section the sequential order of combining of data, PN sequence and carrier does not matter. This fact is exploited in the demodulation section to the advantage of this design.

The incoming signal is applied to the X1 input of an AD534JD while the punctual PN sequence is applied to the Y1 input. The identical wiring configurations (as discussed for the modulation section) for both the interfacing of the PN sequence and the application of the AD534JD are used in the demodulator. However, the incoming signal is applied to the AD534JD as

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opposed to using the 245.7 kHz IF carrier generated in the demodulator. The mixer configuration for the demodulator is located as Figure B.7 in Appendix B.
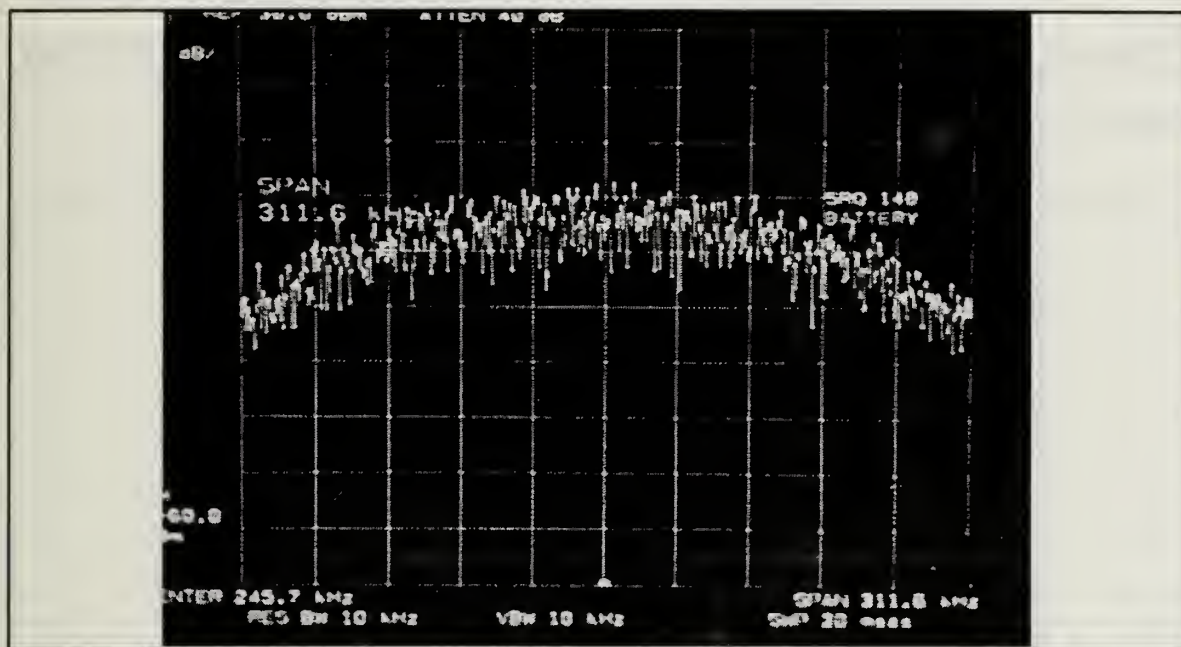
Figure 2.10b: Main lobe frequency spectrum of the transmitted
signal with $(\sin(x)/x)^2$ noise distribution.

At the moment that the channel is connected and a signal is present the instantaneous output of the mixer is one of two things. Either the punctual PN sequence immediately lines up chip for chip with that of the PN sequence used in the modulation process or it does not. In the first case, the output from the AD534JD is a BPSK modulated signal where the phase changes are the result of data transitions only (e.g. a phase change at a maximum of once every 833.33 μsec). The second case is a BPSK modulated signal in which the phase changes are the result of two identical but out of phase PN sequences (phase changes occur at a minimum of each occurrence of a chip period or at least every 6.5104167 μsec). The two cases can be said to be divergent. That is to say that in the first case, where the phase changes are due solely to the modulating data, the signal is approaching coherent demodulation with one less degree of

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randomness. In the second case, the signal is approaching noise with one more degree of randomness and, as a result of the misalignment of the PN sequences, causes further spreading of the already widened frequency spectrum. The difference between the above two cases is what the demodulation section in this design is constructed to exploit.

Figure 2.11:
Top: PN sequence used in modulation.
Middle: Punctual PN sequence from demodulator.
Bottom: Output of the narrow band, band-pass filter.
Note: The PN sequences are approximately 1 chip out of phase yielding a diminutive and varying envelope.

By connecting the output of the AD534JD to a narrow band, band-pass filter (with a high Q), the output of the filter is seen as a small envelope when compared to the output of the filter when correlation of the punctual PN sequences occurs. These outputs are depicted in the Figures 2.11 and 2.12. The resulting signal waveform in Figure 2.11 is representative of each location along the punctual PN sequence in which the alignment difference is greater than 1/2 chip. There is therefore a band of relative correlation that exists that is within 1/2

chip either early or late relative to the punctual sequence. Alignment of the modulation and demodulation PN sequences can be shown to occur in this region. This is demonstrated in Figure 2.12.
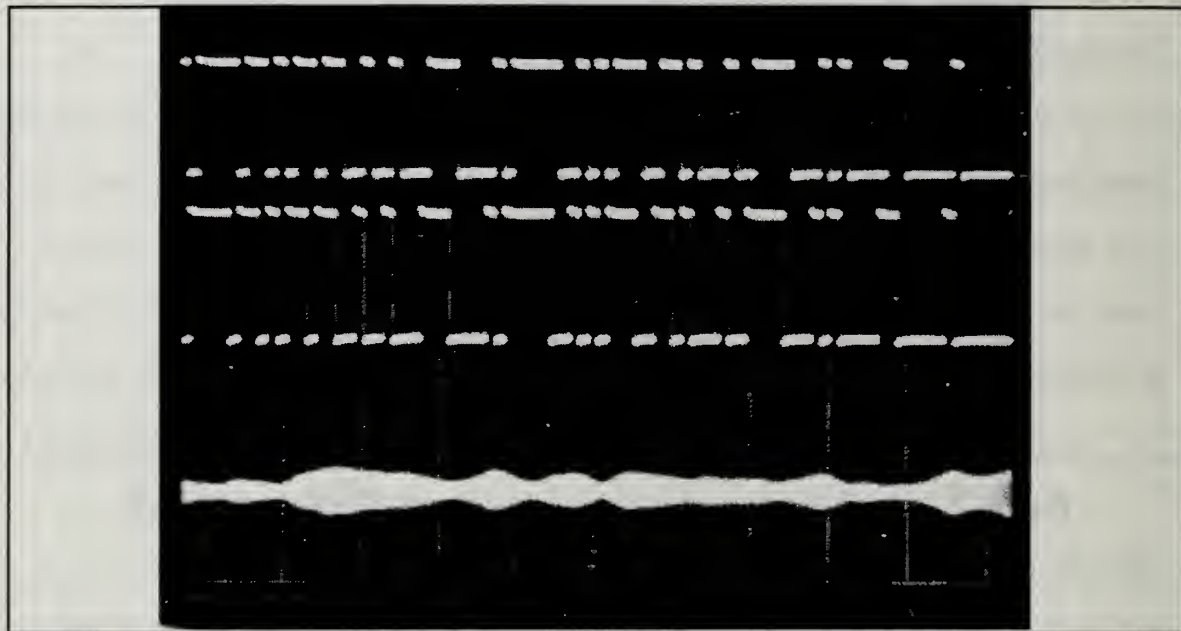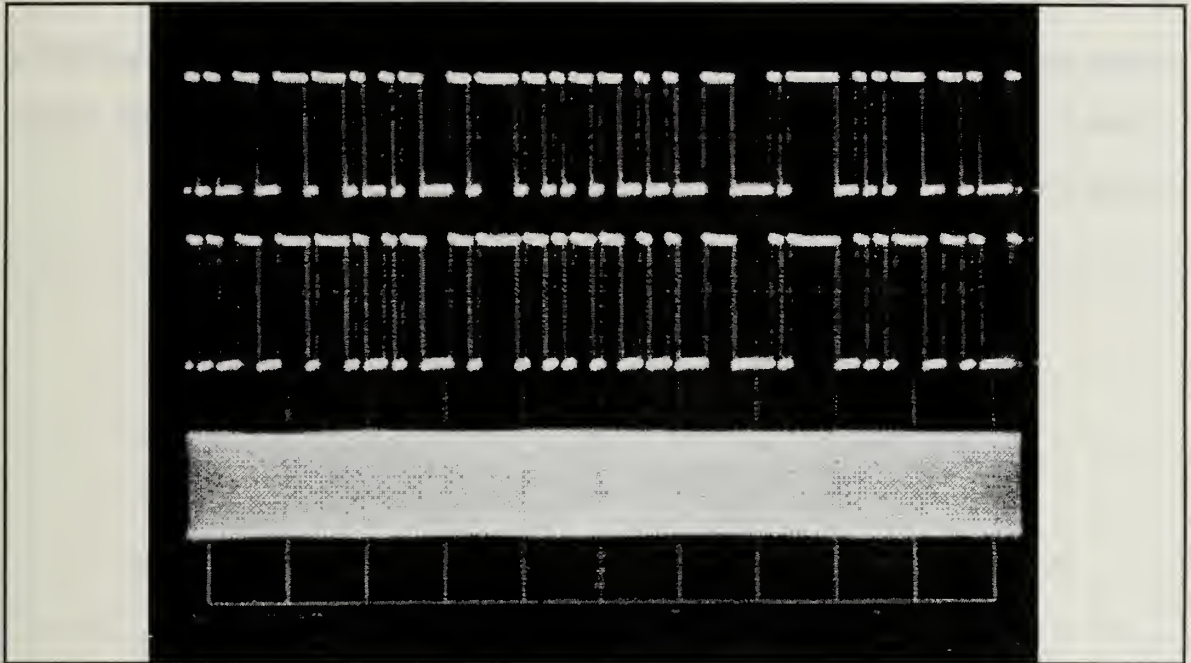

Figure 2.12:
Top: PN sequence used in modulation.
Middle: Punctual PN sequence from demodulator.
Bottom: Correlated output from narrow band, band-pass filter.
Note: PN sequences are in phase yielding a constant envelope.

The output of the mixer is sent through an envelope detector and when the incoming signal is not correlated the output is rather low (approximately 0.1 volts). The output from the envelope detector is notably greater when encountering a correlated signal and consequently, outputs a higher voltage (approximately 0.65 volts) when the incoming signal and the punctual PN sequence are correlated. This higher output is used as the indication of acquisition of the incoming signal and serves to trigger the change from acquisition to track mode. A difference in correlated versus uncorrelated signals can also be seen in the analysis of the spectral outputs of the band-pass filter for

each case. Figures 2.13a and 2.13b show the uncorrelated and correlated spectra as they appear on a spectrum analyzer from the output of the band-pass filter of the punctual channel. Notably, the side lobes of the spread spectrum signal are missing in the uncorrelated output of the band-pass filter since they are attenuated by the high Q of the filter [Ref.2:p.245]. They occur at frequencies centered approximately 1 and 1/2 times the chip rate above and below the center frequency of 245.7 kHz.
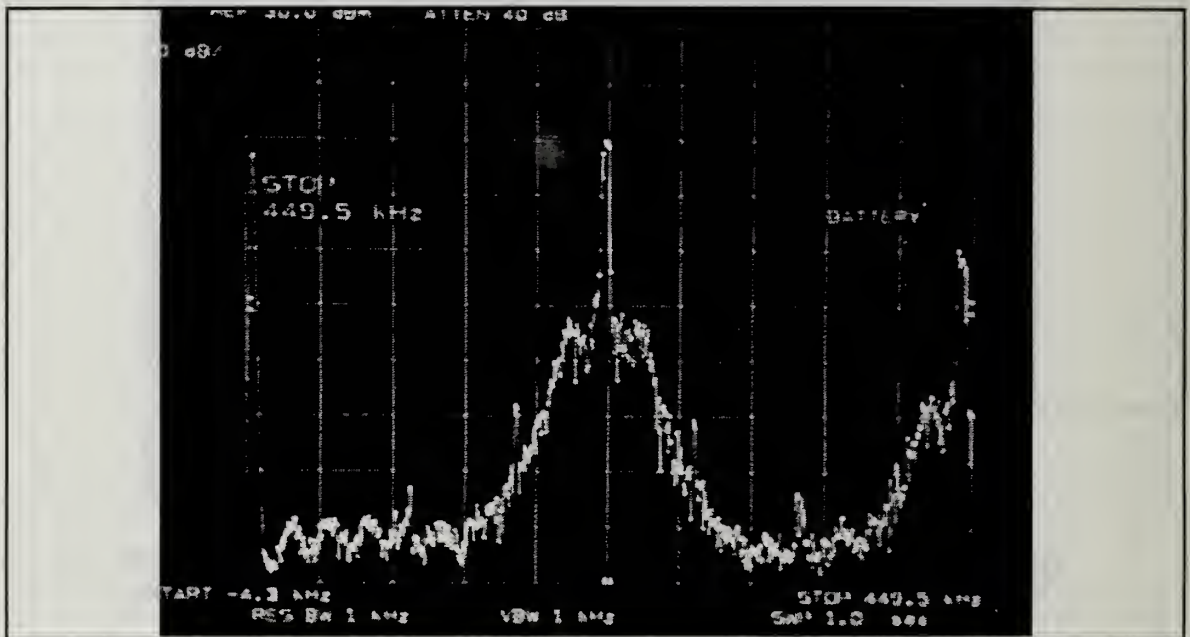
Figure 2.13a: Uncorrelated spectrum output of the punctual channel band-pass filter.

In the uncorrelated signal, the side lobes appear at frequencies about 228 kHz above and below the center frequency of the main lobe. Hence they do not appear at the output of the band-pass filter. Conversely, when correlation occurs the output spectrum of the band-pass filter changes significantly.

The side lobes that appear in the output during correlation are representative of the data-only, BPSK modulated carrier. In fact, the spectral distance between the center frequency of the main lobe and the side lobes in the

correlated case is approximately 1 and 1/2 times the data rate vice the chip rate which, of course, corresponds to a factor of 127 times less. Thus, the data may be recovered from the correlated signal since the indication that the sequence is correlated comes directly from the output of the band-pass filter.
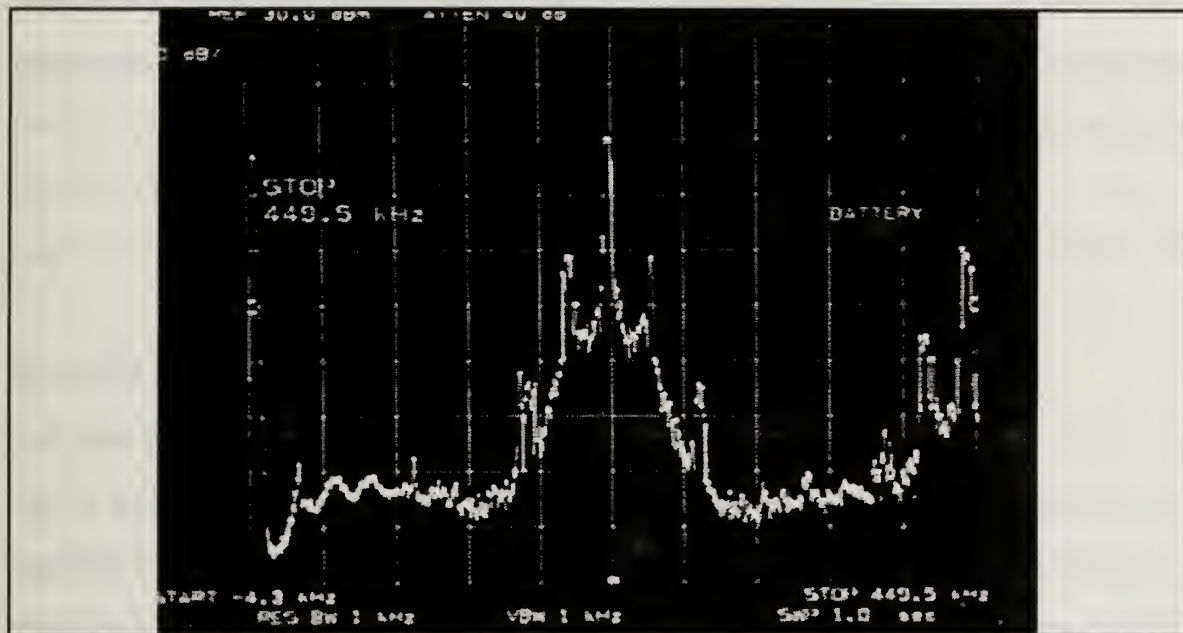
Figure 2.13b: Correlated spectrum output of the punctual channel band-pass filter.
Note: Side lobes appear at approximately 12 dB higher than the remaining noise passing through the band-pass filter.

The mixers employed in the early and late portion of the demodulator section function in the same way as that of the punctual channel. They are consequently configured in exactly the same manner with comparators interfacing the early and late PN sequences and aligned as discussed earlier in the modulation section. Likewise the sinusoidal input is applied exclusively to the X1 inputs and the PN sequences are connected to the Y2 inputs to ensure proper operation. Their respective outputs are also fed through band-pass filters of identical configurations to that which is used in the punctual channel. The early

and late channel filter outputs are each connected to envelope detectors. The envelope detector outputs are used in the tracking of the incoming signal and maintain correlation for the punctual channel by controlling the frequency of oscillation of the crystal oscillator. Clearly, the employment of suitable filters in this application is key to the success of the overall performance. The discussion of feedback control of the VCO is contained in section G of this chapter and follows the discussion of the construction of the band-pass filters.

F. BAND-PASS FILTERS

1. General

The purpose of the filters in the demodulation section of this design is two-fold. They need to provide sufficient filtering to help eliminate noise that may interfere with the proper demodulation of the incoming signal in spite of the relative noise immunity characteristic of SS systems in general. As a by-product of the narrow band filtering characteristic they provide the indication that signal has been acquired as well as an indication of relative phase coherence to the incoming signal.

Cost and component availability are also concerns. To this end the design of the filters here dictates an active filter realization using operational amplifiers. Although a majority of the power consumed in this design is attributed to the operational amplifiers that make up the band-pass filters, aspects of this solution may be viable for ground station applications where the power consumption of the modem is not a concern. Clearly, passive elements such as crystal filters will be used in a final design due to limited spacecraft power. Nonetheless, the characteristics of the design remain the same and, as a matter of practicality, the use of operational amplifiers here allows for proof of concept in this design.

2. Technical

The basis for the design of the band-pass filters is taken from References 11 and 12. The circuit diagram is located in Appendix B as Figure B.8. The operational amplifiers employed to construct the filters are LM318N operational amplifiers. The identical power supply bypass capacitance requirements as mentioned in section D.2 of this chapter are applied here and are essential for proper operation of the filters. Appendix C contains a computer program and set of MATLAB generated, filter response curves showing nearly actual characteristic pass bands for the filters in this design [Refs.11 & 12].

G. VCO FEEDBACK CONTROL

1. General

The primary concern in an operational spread spectrum system is to ensure that the demodulator can convert the incoming signal from the broad spectrum of frequencies over which the spread signal covers to a narrow band signal from which the original transmitted data may be recovered. To accomplish this a demodulation design must possess two critical features. First, the same PN sequence must be used in the demodulation process as was used to originally encode the data in the modulation process. Second, the frequency at which the demodulation PN generator is clocked must be controlled and compensated for differences between it and the PN sequence imbedded within the incoming signal. Additionally, the frequency control must be agile enough to compensate for changes in the incoming frequency to include the potential Doppler shifts associated with low earth orbiting satellite communications. Upon close examination, the ability of the design contained here obviously does not posses the VCO frequency agility required for an operational satellite. The type of system employed here, however, realizes the fundamental operating principles

necessary to achieve the desired final design objectives. This design proposes a means of frequency control which takes the form of a delay lock loop [Ref. 1:p. 253].

2. Technical

The output of the AD534JD mixers for the early and late correlation channels take the same form as the output of the punctual channel as discussed in the previous section. These early and late correlation signals can clearly be seen as maximum when each of the respective PN sequences is in correlation with the incoming signal.
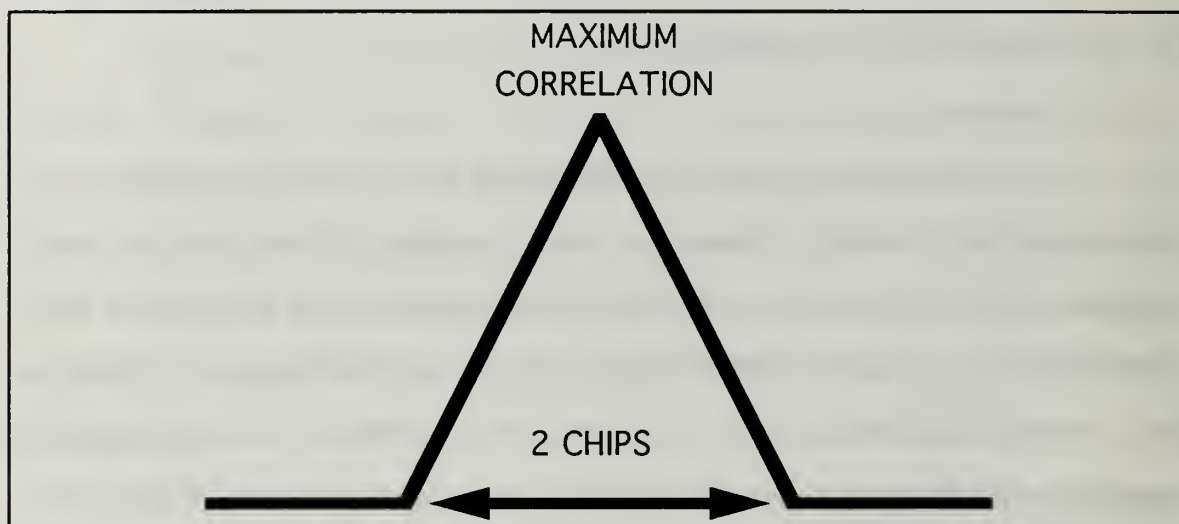
Figure 2.14a: Ideal correlation triangle.

As any one of the PN sequences begins to come into within one chip of correlating with the incoming signal, the output of the associated envelope detector begins to rise linearly from the uncorrelated output value to the maximum value achieved when the PN sequences are exactly correlated. Beyond the maximum value, as the PN sequences pass one another, the envelope detector output falls to the value corresponding to that of an uncorrelated signal. These correlation signals are represented as triangular pulses which occur at a frequency

representative of difference between the incoming signal and the demodulator PN sequence. This triangular pulse is known as the correlation triangle [Ref. 1:p.254]. A representation of an ideal correlation triangle for the punctual channel is shown in Figure 2.14a.
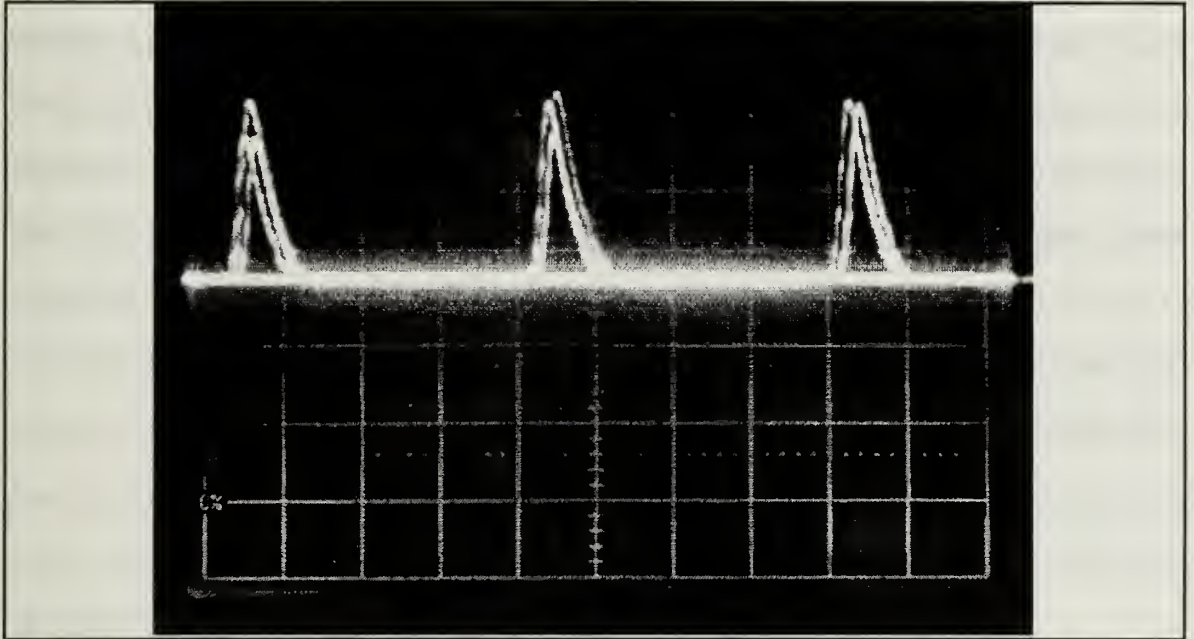
Figure 2.14b: Punctual channel correlation triangle.
Oscilloscope settings: X = 0.1 msec/Div., Y = 5 v/Div.

The width of the triangle at its base is simply related to the overlap distance of two like PN sequences and is therefore two chips wide. This is the ideal case. The actual correlation triangle for this design is slightly narrower due to the response of the system and the purity of the signals employed. It is also slightly rounded due to the bandwidth restriction of the demodulator band-pass filter [Ref.1:p.21].

Even though the output taken from this design is clearly not an ideal case, the correlation triangle remains useful in both the acquisition and tracking applications carried out in the demodulator. The actual correlation triangle for the

punctual channel is shown in Figure 2.14b. The early and late correlation triangles are identical in appearance but are not shown in the figure.

There are also secondary correlations associated with the portions of the sequence that match for several bits of the two PN sequences. These secondary correlations create correlation triangles of lesser magnitude than that of the truly correlated position in the PN sequence [Ref.1:p.76]. Hence, when a strong secondary correlation occurs the potential for the circuit switching from acquisition to track mode exists. However, soon after track mode has been established the PN sequences will no longer be correlated and the system will return to the pre-acquisition or search mode until the next correlation is reached. The threshold voltage in this design is set sufficiently high to prevent secondary correlations from introducing any notable degradation in performance.
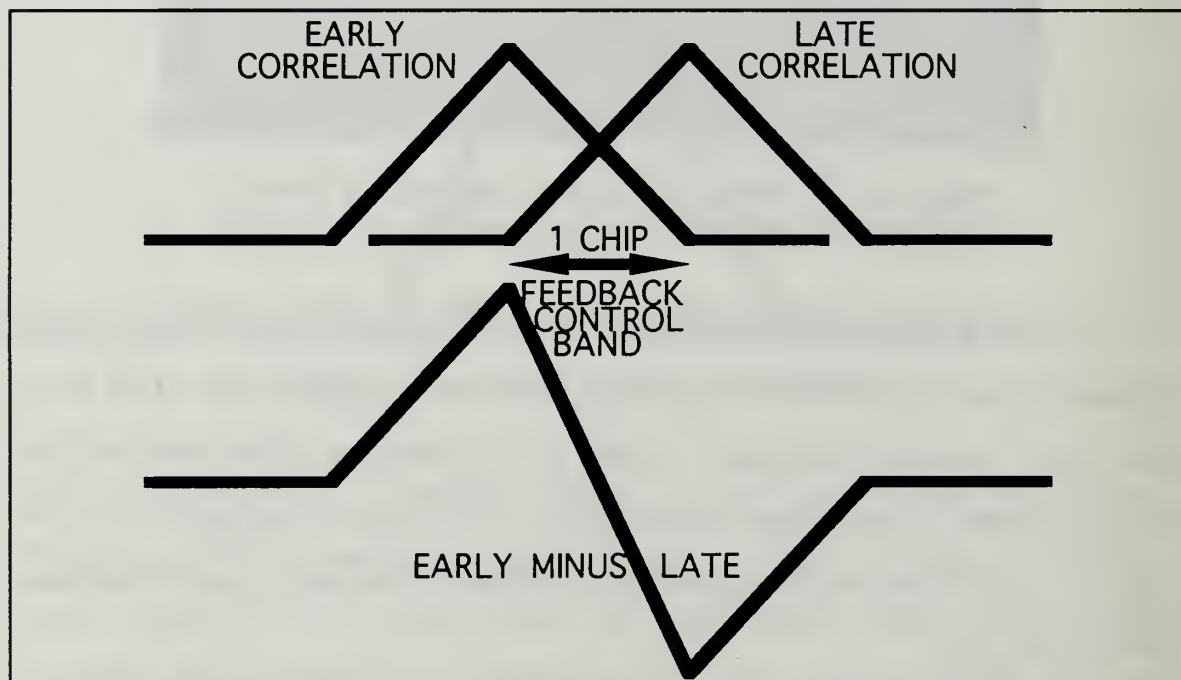

Figure 2.15: Ideal Early minus Late correlation signal.
Note: The control band is one chip wide.

The timing delays used to establish the early and late PN sequences allow for the creation of a linear voltage control zone for use in feedback control. The voltage generated by the early minus late (E-L) circuitry during operation in the track mode is applied to the varactor diode. This in turn adjusts the oscillator frequency by changing the coupling capacitance seen by the crystal. The outputs of the early and late envelope detectors are amplified using standard non-inverting amplifier configurations employing LM318N operational amplifiers [Ref. 5:p.59]. The output of the late correlation signal is then inverted and added to the early correlation signal thus creating an E-L correlation triangle pair. The ideal E-L correlation signal is shown as Figure 2.15.

In order for this feedback voltage to be useful in any spread spectrum design the punctual signal must be within 1/2 chip of maximum correlation. And for what may now be obvious reasons, any frequency adjustments made by this correction voltage will be entirely erroneous unless the punctual channel has first acquired the incoming signal.

When there is no incoming signal the demodulator is in the search mode. The VCO operates at a constant frequency based on the static control voltage supplied to the varactor diode via the 100KΩ potentiometer. The division chain is configured to output the PN generator clock at a frequency of 163.84 kHz.

From the point at which transmission of a signal commences, the output of the punctual correlation channel is monitored by means of its associated envelope detector and an amplifier. The acquisition phase of signal demodulation utilizes a sliding correlator [Ref. 10:p.240]. The concept noted in this reference is employed here but the circuit is drastically different. As the PN sequence slides through the incoming signal variations in the demodulated envelope are sent to a comparator. When correlation occurs the envelope detector output voltage rises. The threshold voltage on the LM311P employed to mark the point of punctual

correlation is set to change the comparator output from low to high when the output of the punctual channel envelope detector goes sufficiently high.

The difference in frequency of the PN sequence associated with the incoming signal and the PN sequence of the demodulator in the acquisition mode is 10.24 kHz. If the arrival of the incoming signal coincides exactly one chip past the potential synchronization point, a maximum of 126 chips must be traversed by the demodulator in order to acquire the signal. For this design the resulting theoretical maximum time to acquisition is 12.3 msec which corresponds to 14.765 information bits. Once the punctual correlation signal is detected the control voltage input to the VCO is switched. This is accomplished by using an analog switch (PWI SW06) triggered by the punctual correlation signal itself via the LM311P comparator. The incoming signal is then acquired. The circuit diagram for the feedback control section is shown in Appendix B as part of Figure B.5.

The threshold voltage for switching is set to minimize secondary correlations. It must be low enough though to account for reduced correlation triangle peak magnitude induced by the 10.24 kHz frequency differential when the device is in the search mode of operation. Once the SW06 is activated the static control voltage is replaced by a sum of the original control voltage and the input from the E-L amplification stage. When a frequency difference exists the punctual PN sequence will attempt to drift (early or late) out of correlation if a correcting voltage is not applied to the VCO. Upon drifting from the maximum correlation value the early or late correlation signal (depending upon the direction of drift) will correspondingly add to or subtract from the control voltage sensed by the VCO. The VCO will then adjust the frequency of oscillation until the frequency that matches the maximum point of punctual correlation is reached. This feedback continues throughout the receipt of the incoming signal and the

demodulator is thus maintained in a tracking mode and may further translate the incoming signal back into the data bits that were transmitted.

H. DATA CONDITIONING

Once the received signal has been acquired, the PN sequence imbedded in it has been stripped from the carrier by nature of the acquisition process described earlier. Consequently, the simple addition of the function generator carrier (generated in the demodulator) with the BPSK signal produces an additive (high voltage value) resultant output for data that was transmitted as a logic "1" and a cancellation of waveforms occurs for data that was transmitted as a logic "0".
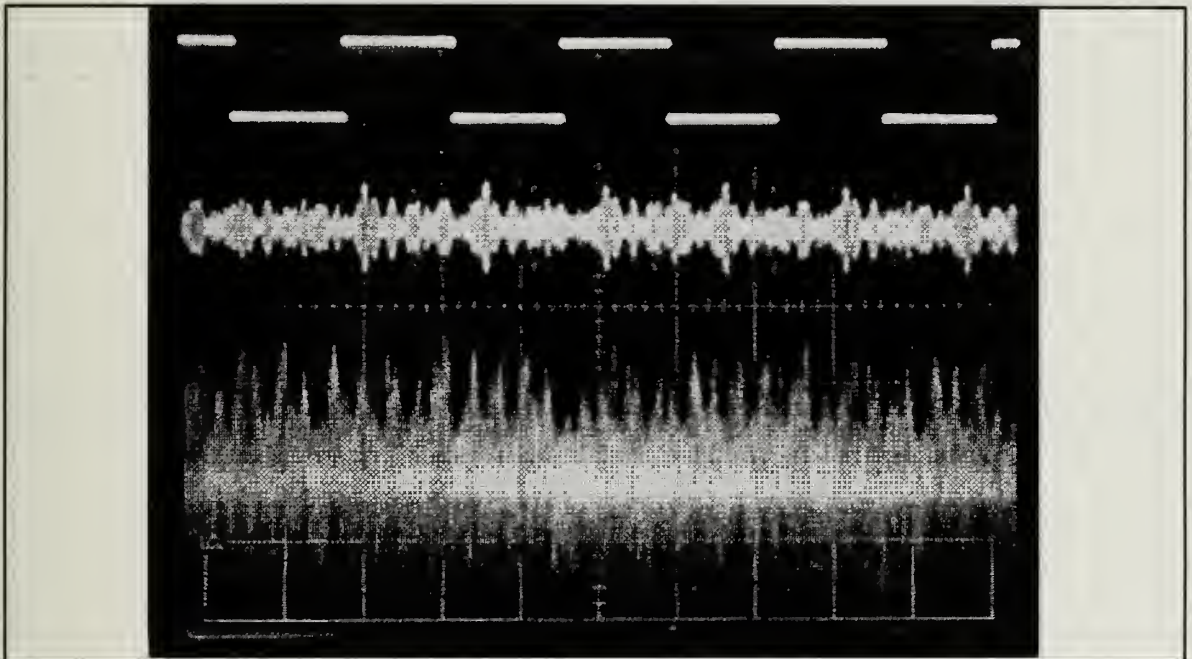

Figure 2.16:
Top: Transmitted data.
Middle: Uncorrelated received waveform.
Bottom: Unconditioned uncorrelated data waveform
output from the uncorrelated punctual channel(noise).

The resulting waveform is a BPSK modulated signal that contains the transmitted information and is ready for further demodulation.

Since the PN generator and function generator clocks are derived from the same source, the phase coherence of the sine-wave generated in the demodulator is already established relative to the incoming signal phase. This of course holds true only if the tracking feedback voltage maintains an in-phase relationship with respect to the punctual PN sequence.

When the signals are not correlated the output of the demodulator is essentially noise since no form of data is distinguishable from the output. The waveforms associated with an uncorrelated condition are shown in Figure 2.16. Conversely, when correlation occurs, the output clearly depicts the presence of data. The BPSK modulated signal produced during track mode and the unconditioned recovered data signal are shown in Figure 2.17.
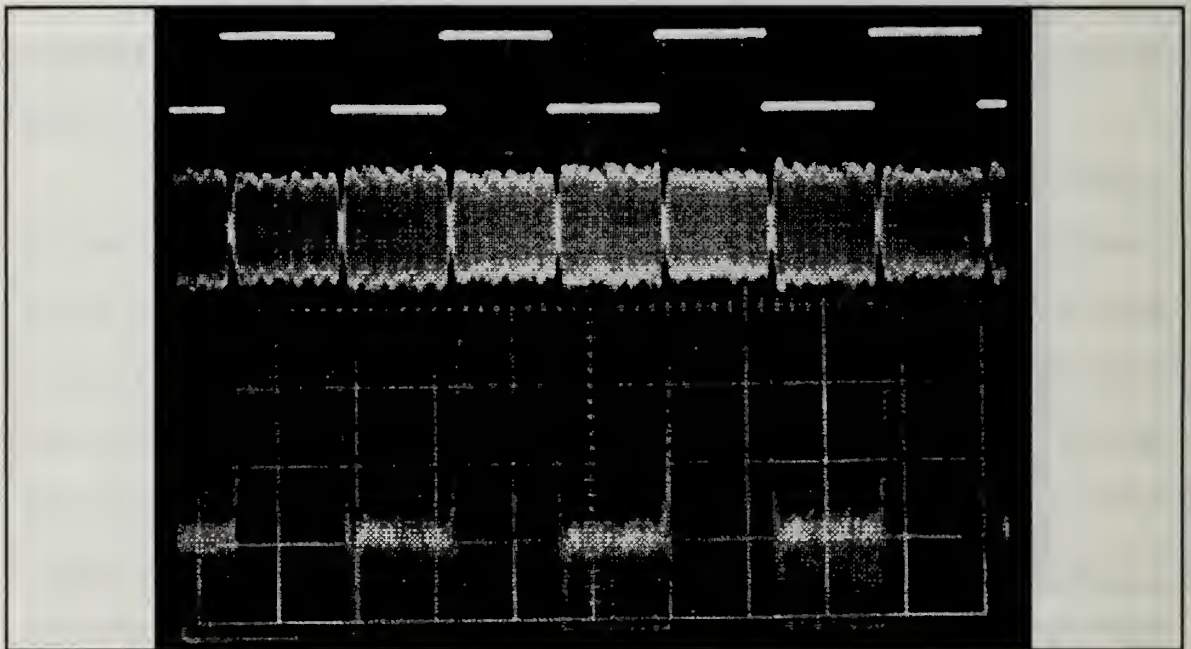

Figure 2.17:
Top: Transmitted data (600 Hz square-wave).
Middle: Correlated BPSK wave form
(data modulated PN sequence stripped).
Bottom: Demodulated unconditioned data.

The carrier generated in the demodulator is added to the BPSK demodulated signal and the result is amplified and passed through an envelope detector. The partially conditioned data stream is then sent to a comparator which brings the voltage levels back to their original TTL values. The resultant fully conditioned data is depicted in figure 2.19 and the circuit diagram is located in Appendix B as Figure B.10.
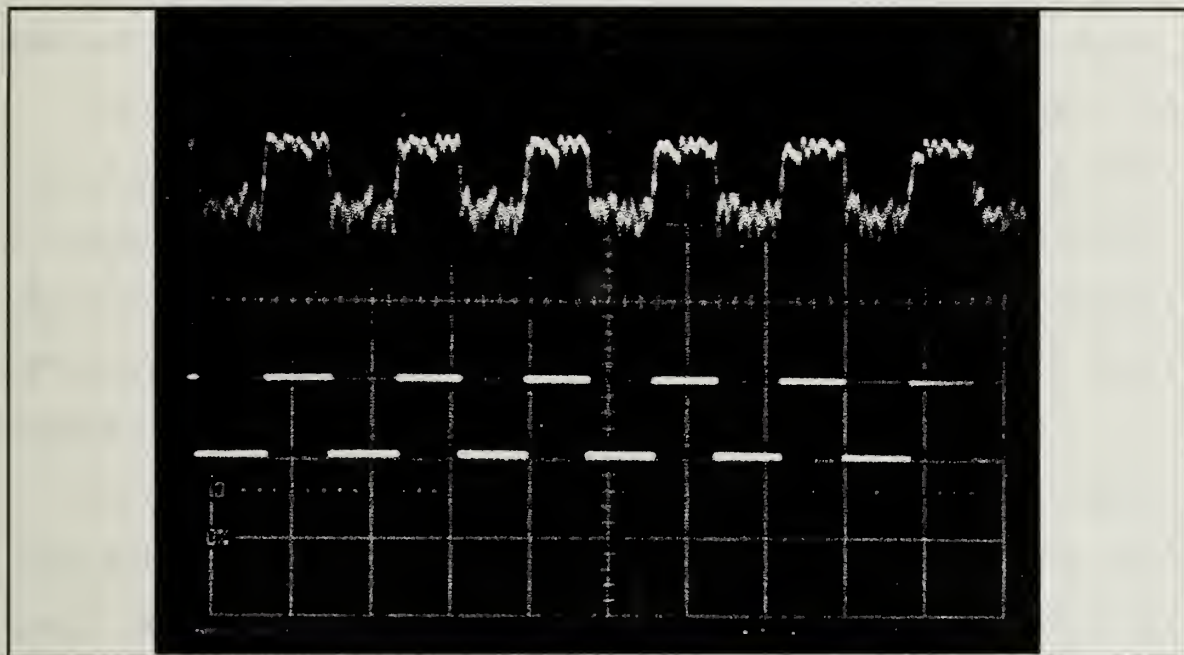
Figure 2.19:
Top: Demodulated data signal, partially conditioned
(amplifier Gain = 50) DC offset = 7.3 volts.
Bottom: Fully conditioned data restored to
600 Hz TTL compatible voltage level.
Oscilloscope settings: X = 0.1 msec/Div. , Y = 5 volts/Div. .

Doppler shifts supported by this design are minimal (approximately 5 Hz at the chip rate of 153.6 kHz). This is of course due to the nature of the VCO (inherently stable) and the minimal effect of the small range of capacitance over which the varactor diode changes during feedback control. A more sophisticated VCO is clearly called for in future design work considering the total Doppler shift expected for PANSAT. However, the design described here remains consistent in

operation and can be improved using more sophisticated components in the same applications as are developed here. Additionally, any significant Doppler shift encountered in future applications of this design will require the addition of a buffer in order to reestablish the 1200 bps data rate into the any interfacing device.

III.   CONCLUSIONS

A.   GENERAL

The basis for this design comes from a broad spectrum of literature that for the most part deal with the theoretical aspects of communications systems. A large part of the development of the modem design contained here is the result of trial and error using available components for functional realization of the design.

The modem performs extremely well in laboratory IF loop-back testing. The only bit error rate testing performed consists of the measurement of output data compared to input data using the IF channel signal alone with no additive noise. This is not a substantially rigorous testing procedure and as expected the bit error rate is significantly lower than the performance requirement dictated by the PANSAT design specifications.

The requirement for PANSAT dictates a bit error probability of 10^{-6} or less. Tests under various levels of additive noise will be needed to validate the final design but are not conducted for this design. The final design will be modified for operation over an RF channel and will require greater frequency agility than demonstrated here. Therefore, any additional bit error rate testing will clearly be more meaningful when implemented on the RF design. Additionally, a fading channel should be simulated to evaluate the overall performance of the final modem design.

B.   TECHNICAL

1.   Circuit Sensitivity

The feedback voltage to the oscillator cannot be measured during operation if tracking is expected to be maintained. Any device connected to the center tap of the potentiometer used to establish the dwell point for E-L feedback

will add stray capacitance to the circuit and thereby change the frequency of oscillation. This is due to the small range of the varactor capacitance. Since the varactor diode capacitance range is 22 to 440pf using the full range voltage control of the device it is significant to note that the voltage control band changes approximately 2 volts yielding an overall change in the capacitance seen by the oscillator of about 100 pico-farads. This small control range aids in the tracking process and in this application creates a mildly responsive but sensitive tracking characteristic.

2. VCO Control

The polarity of the controlling voltage used in feedback must be maintained at a level such that the static control-voltage/feedback-voltage sum used in the tracking mode of operation remains a positive quantity. This protects the inverter used in the oscillator configuration. Additionally, the frequency is only controllable if the center tap of the potentiometer is connected to the output terminal of the inverter used in parallel with the 4.9152 MHz crystal. Specifically, if voltage feedback control as discussed here is used in the future design, any difficulties that arise relating to inability to maintain track or complete lack of feedback control are undoubtedly related to a large negative feeback voltage or an improperly wired oscillator circuit (due to an improperly biased varactor). Since it is expected that the VCO used in this design will be replaced in whole these particular problems will be avoided entirely.

3. Power Consumption

Clearly the design as stated is extraordinarily power inefficient and, by today's standards, considering the use of the integrated circuits employed here could be improved significantly. Several modifications to the existing design may be implemented immediately. The obvious ones are the use of CMOS vice standard TTL devices in all digital applications. It is significant to note that in

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many cases in this design the TTL components used are of the least power efficient variety and were chosen based on availability alone. At the very least a power savings could be achieved by converting all 7400 series components to their 74LS00 equivalent components.

Additionally, the threshold voltages established in the analog section are lower than the +5 volt power supply available and since resistance voltage dividers are employed to set these voltages more power is lost by using the +15 volt supply. This can be changed but as mentioned in the design development, many of the analog components used here will be replaced in their entirety by either passive components (crystal filters and mixers) or power efficient amplifiers.

These points are not important as concerns the functionality of the design or in the evaluation of its operational characteristics (power consumption aside). This design, as it is intended, provides a particular solution that is meant to lay the groundwork leading to the final design. Clearly, substantial power savings can be achieved but, for this design the importance lies in the realization of a functional prototype and to this end the design is a success.

APPENDIX   A.

Functional Block Diagrms

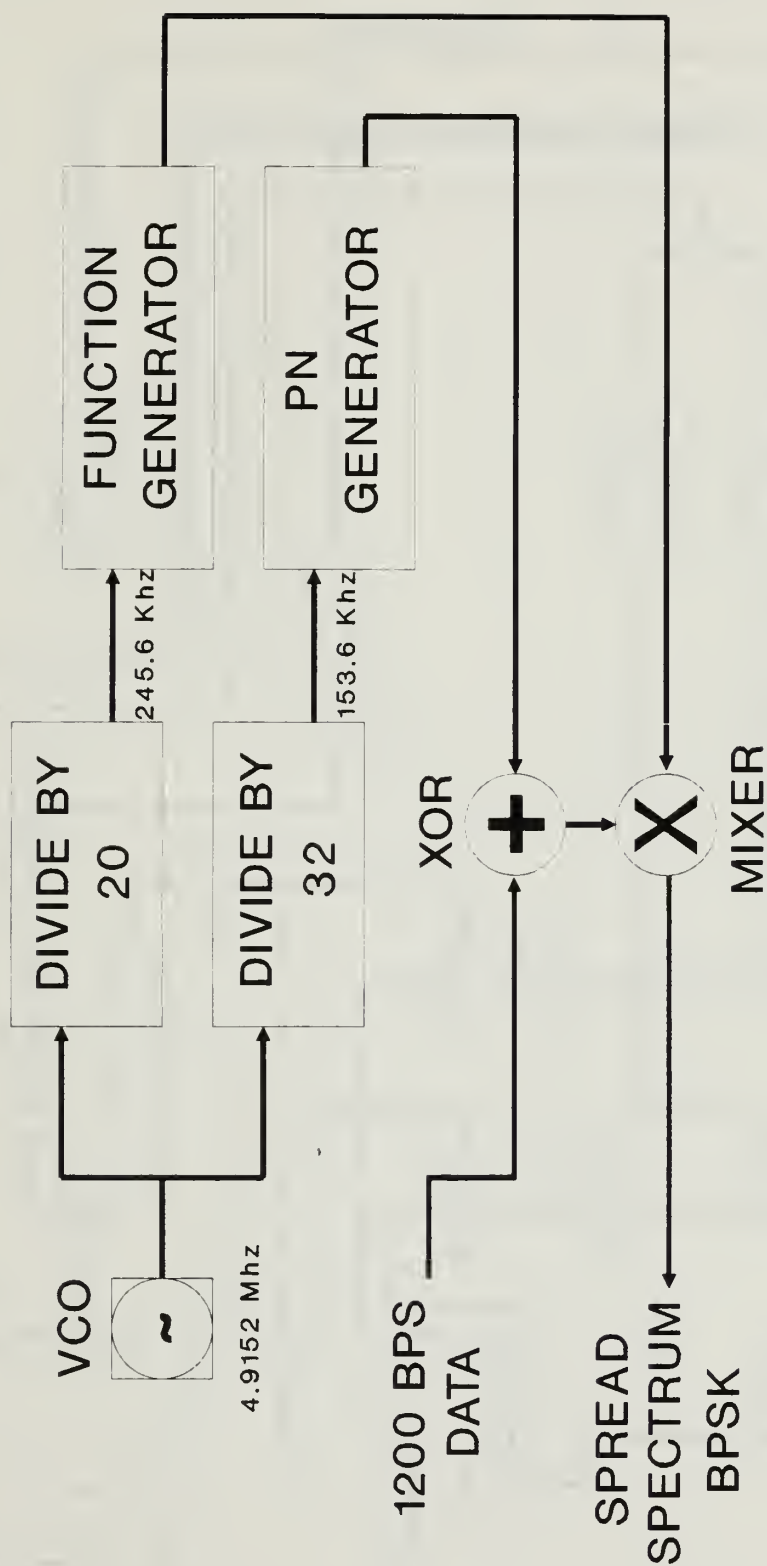# Modulator-funcional block diagram

Figure A.1

49

Demodulator functional block diagram

Figure A.2

50
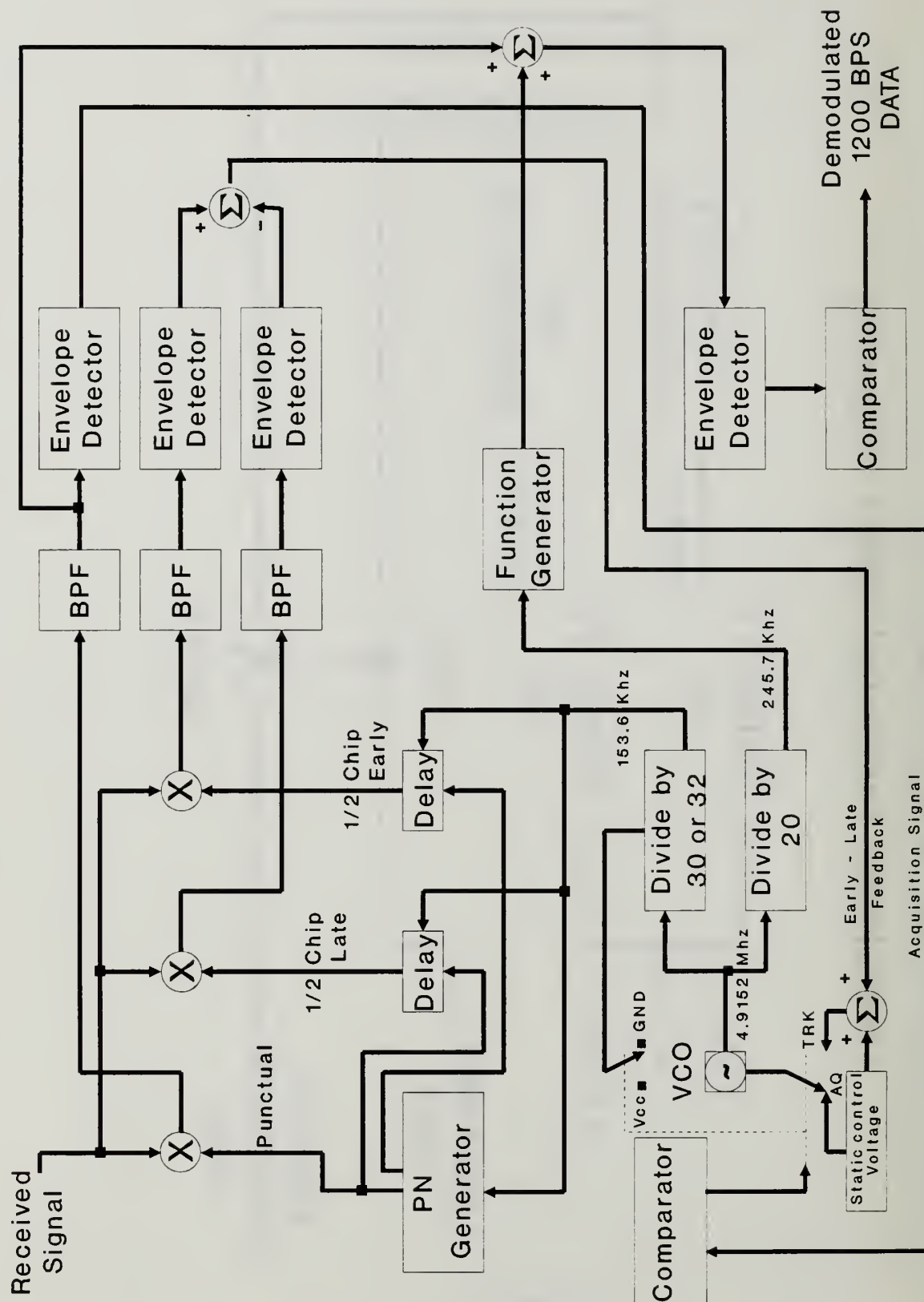
APPENDIX   B.

Circuit Diagrams and Bill of Materials

B.1 OSCILLATOR AND DIVISION CHAIN
(MODULATOR)

Clock to PN generator
153.6 Khz

Square wave to
function generator
245.7 Khz

Divide by 32

Divide by 20

52
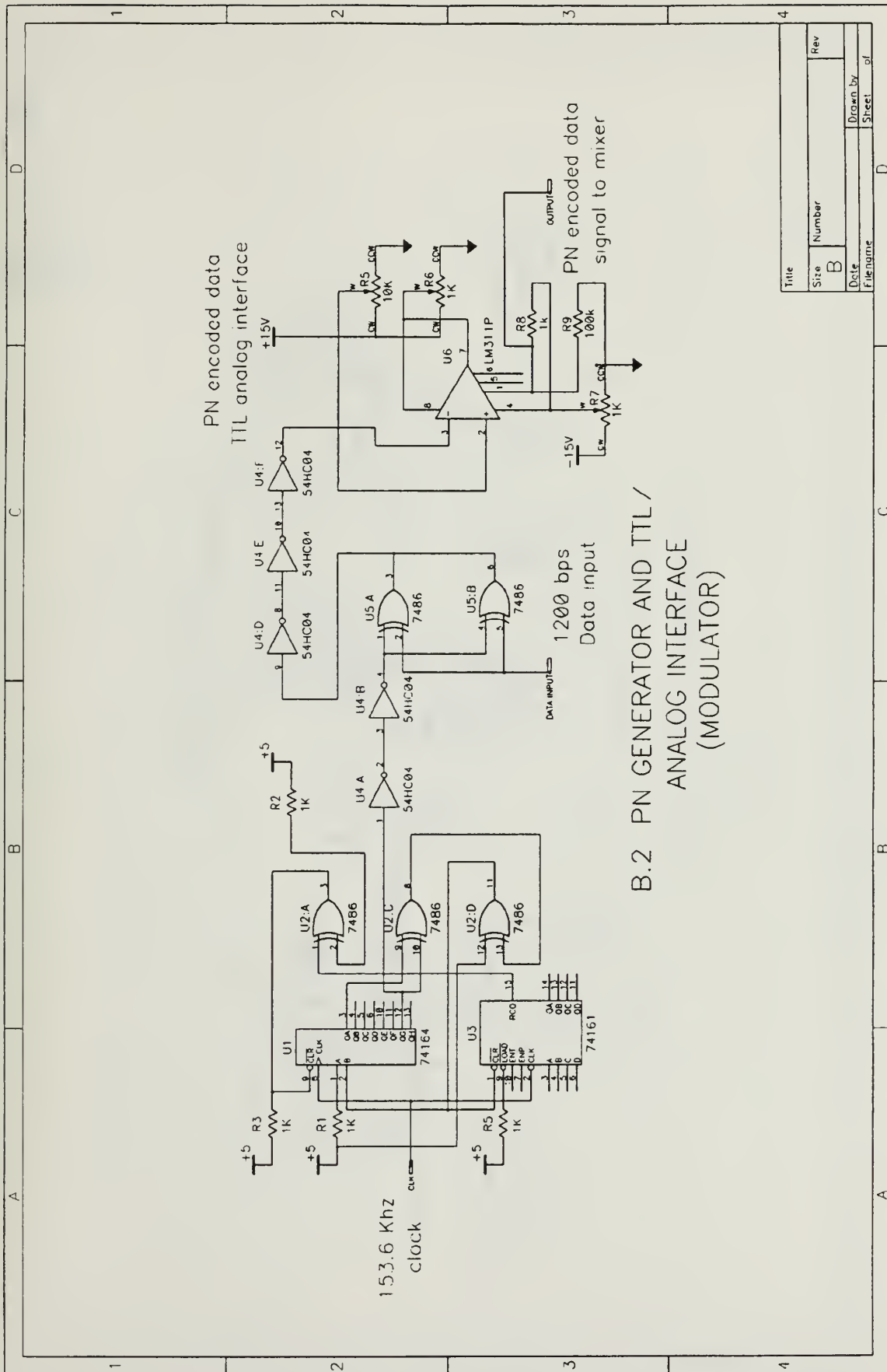
B.2 PN GENERATOR AND TTL /
ANALOG INTERFACE
(MODULATOR)
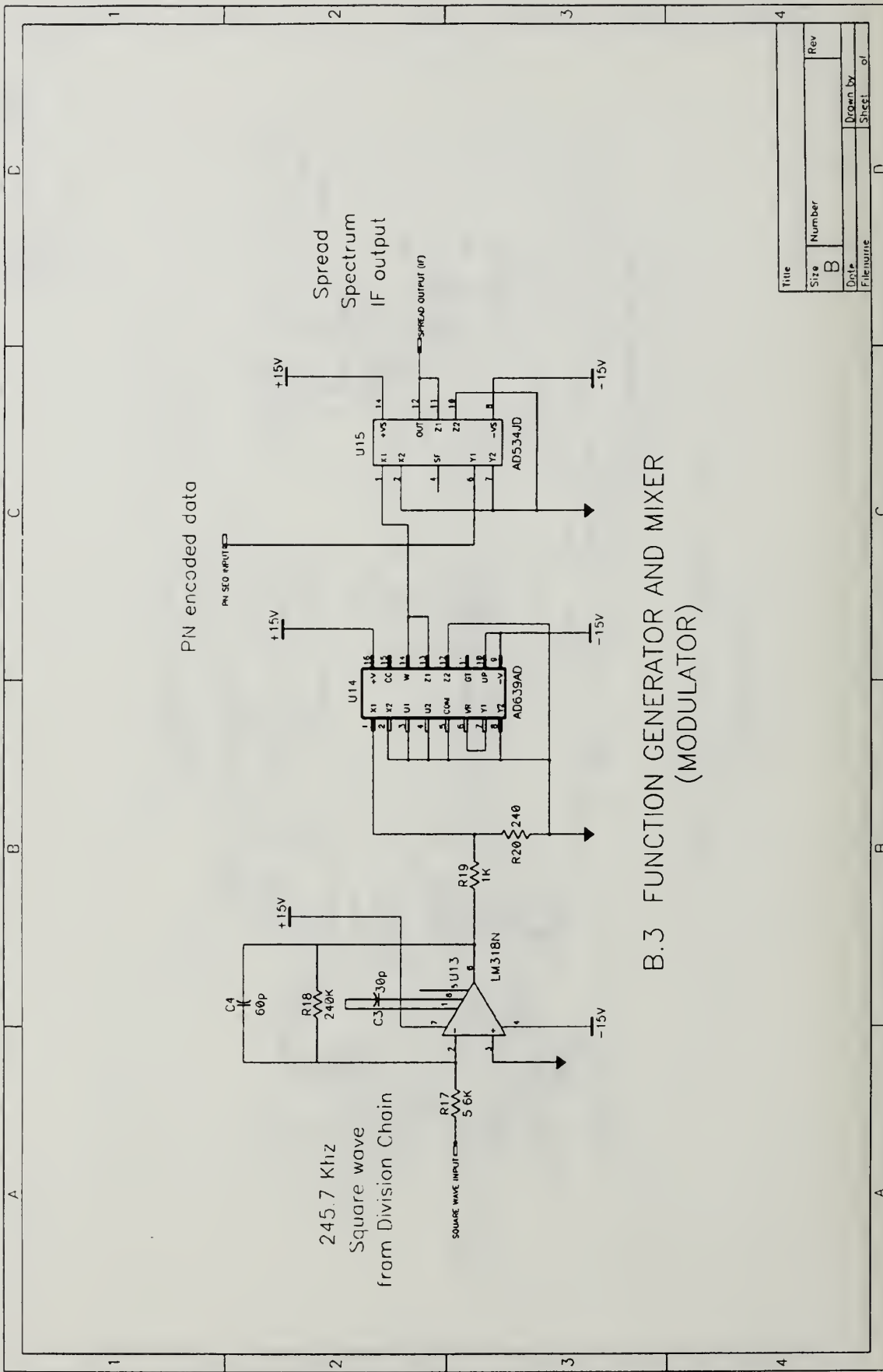
B.3 FUNCTION GENERATOR AND MIXER
(MODULATOR)

PN GENERATOR

DATA IN

OSCILLATOR

DIVISION CHAIN

FUNCTION GENERATOR

SPREAD SPECTRUM
IF OUTPUT

B.4 MODULATOR SCHEMATIC

Divide by 32

Divide by 20

B.5 OSCILLATOR AND DIVISION CHAIN
(DEMODULATOR)

Clock to PN generators
163.84 Khz: Acquisition
153.70 Khz: Track

Divide by 30: Acquisition
Divide by 32: Track

Divide by 20

Square wave to
function generator
245.7 Khz

Punctual correlation
signal from
punctual envelope detector

Early − Late
Feedback Voltage

B.6 PN GENERATOR AND DELAY WITH
TTL/ANALOG INTERFACE (DEMODULATOR)

B.7 DEMODULATOR MIXER CONFIGURATION

B.8 4th ORDER BAND PASS FILTER
(PUNCTUAL CHANNEL DEPICTED)

B.9 EARLY MINUS LATE ENVELOPE
DETECTORS AND TRACKING SIGNAL

B.10 DATA CONDITIONING CIRCUIT

TTL data output

Uncondition data signal input

61
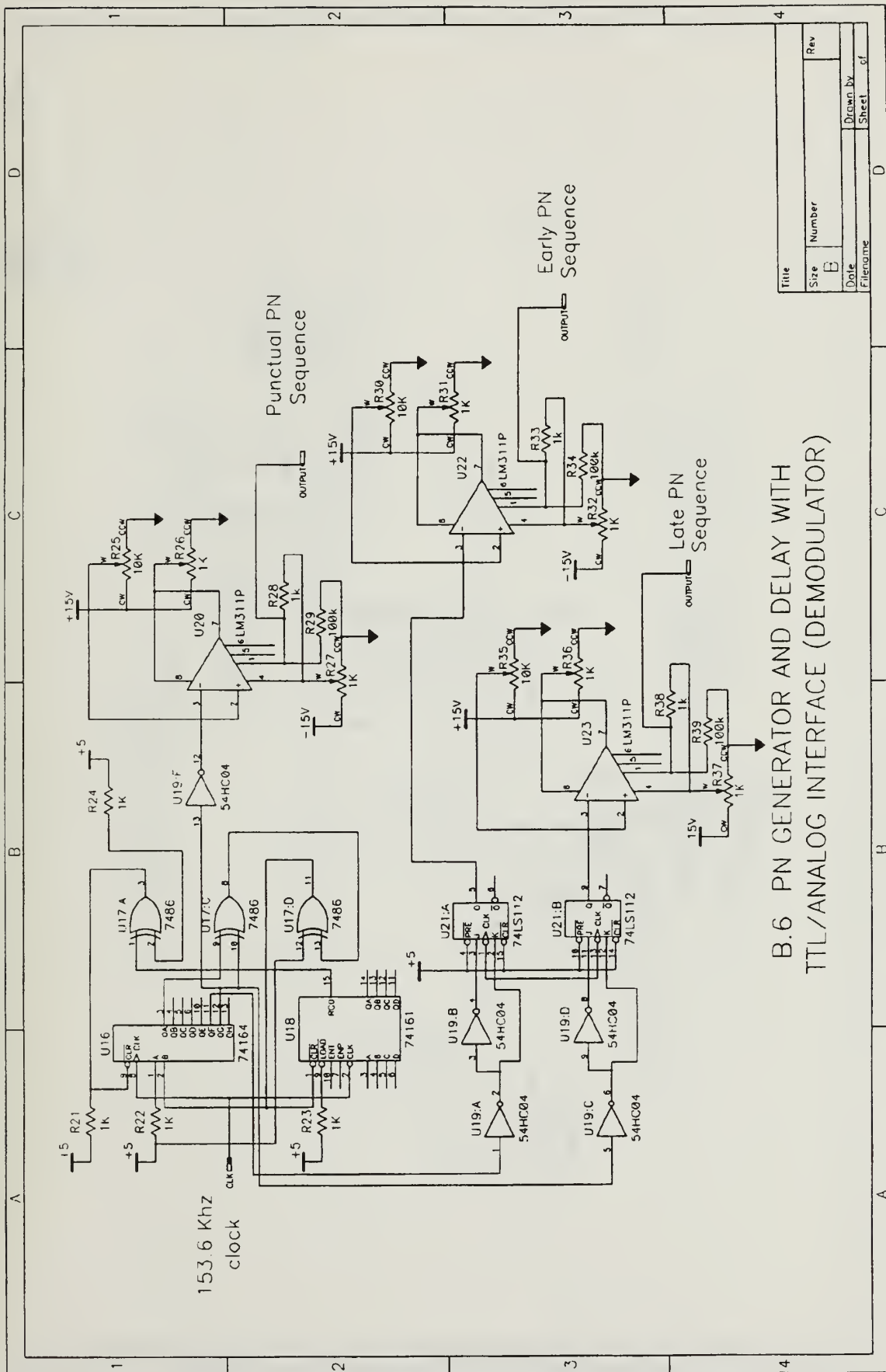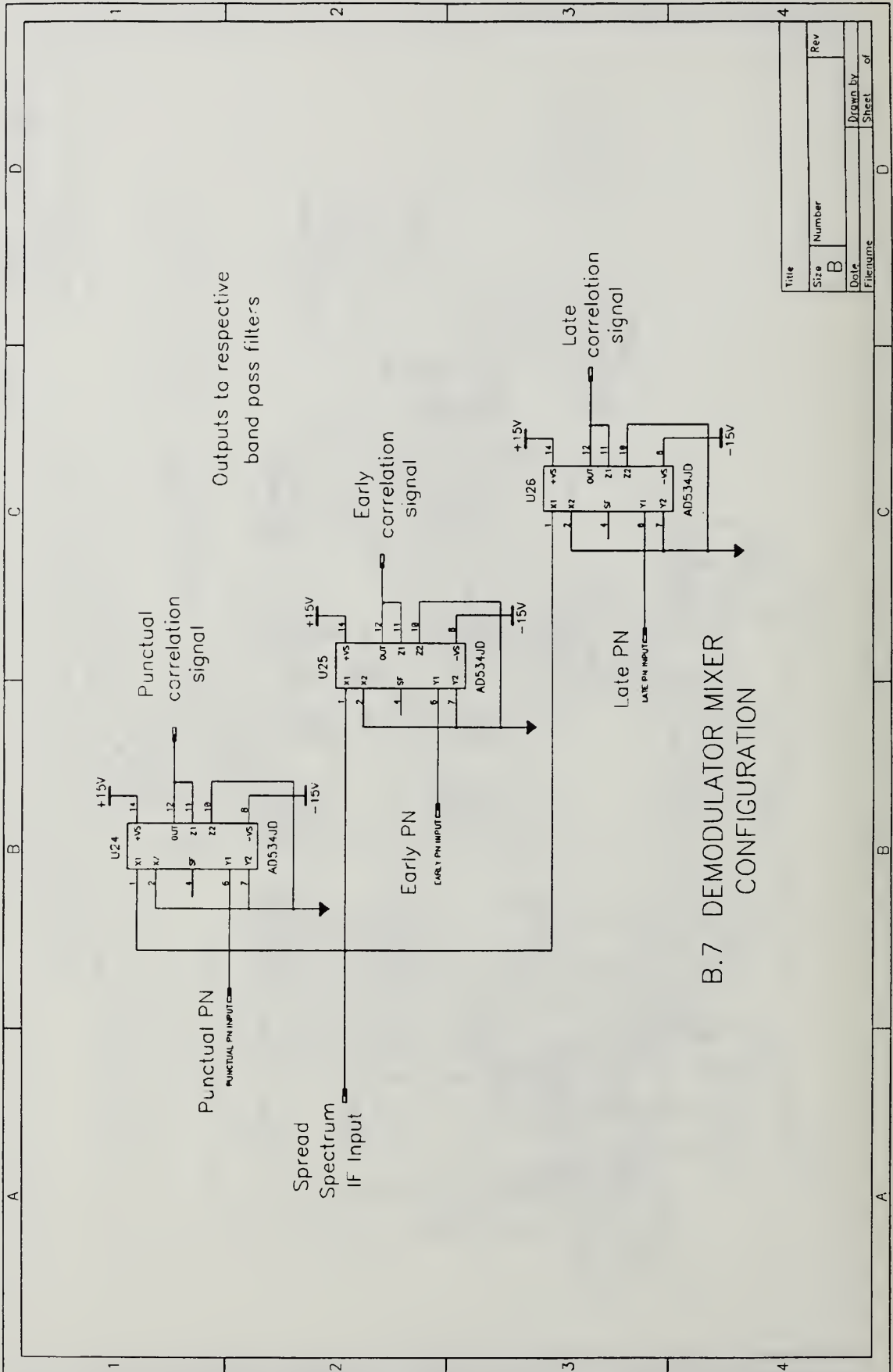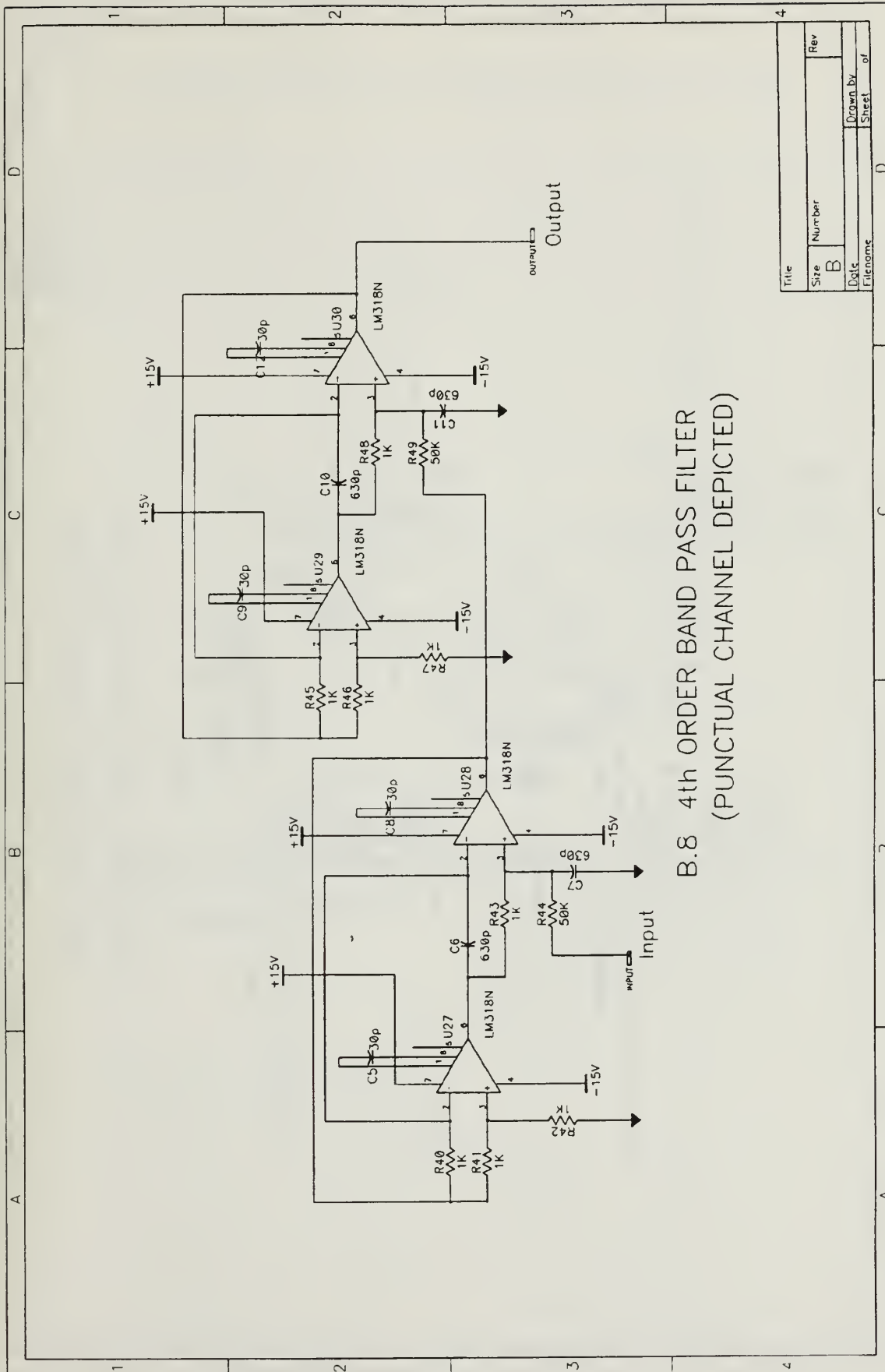
MODEM BILL OF MATERIALS.

SCHEMATIC REPORT

Quantity	Type	Value	Ref. Designators
4	54HC04		U4,U7,U19,U44
2	54HC109		U11,U48
2	54HC112		U9,U46
2	74161		U3,U18
2	74164		U1,U16
4	74192		U8,U10,U45,U47
3	7486		U2,U5,U17
1	74LS112		U21
4	AD534JD		U15,U24,U25,U26
2	CAP	0.1u	C35,C38
3	CAP	1u	C30,C32,C40
18	CAP	30p	C3,C5,C8,C9,C12,C13,C16, C17,C20,C21,C24,C25,C28, C29,C31,C33,C34,C39
4	CAP	47p	C1,C2,C36,C37
1	CAP	60p	C4
12	CAP	630p	C6,C7,C10,C11,C14,C15,C18, C19,C22,C23,C26,C27
2	CRYSTAL	4.9152 MHz	X1,X2
3	DIODE	1N914R	D2,D3,D4
7	LM311P		U6,U12,U20,U22,U23,U49, U51
18	LM318N		U13,U27,U28,U29,U30,U31,

MODEM BILL OF MATERIALS (CONTINUED).

SCHEMATIC REPORT

Quantity	Type	Value	Ref. Designators
LM318N			U32,U33,U34,U35,U36,U37, U38,U39,U40,U41,U42,U50
2	POT	100k	R11,R84
7	POT	10k	R5,R13,R25,R30,R35,R88, R95
12	POT	1k	R6,R7,R12,R14,R26,R27,R31, R32,R36,R37,R86,R87
8	RES	100k	R16,R75,R90,R9,R29,R34, R39,R97
13	RES	10k	R71,R72,R73,R76,R77,R78, R79,R80,R81,R92,R93,R94, R74
1	RES	130k	R70
35	RES	1k	R1,R2,R3,R5,R15,R19,R21, R22,R23,R24,R40,R41,R42, R43,R45,R46,R47,R48,R50, R51,R52,R53,R55,R56,R57, R58,R60,R61,R62,R63,R65, R66,R67,R68,R89R8,R28, R33,R38,R96
2	RES	1M	R10,R83
1	RES	240	R20
1	RES	240k	R18
2	RES	30k	R82,R85
1	RES	5.6k	R17
6	RES	50k	R44,R49,R54,R59,R64,R69

MODEM BILL OF MATERIALS (CONTINUED).

SCHEMATIC REPORT

Quantity	Type	Value	Ref. Designators
1	RES	550K	R91
1	SW-06		U43
2	VARACTOR	22-440pf	Q1,Q2

Total Parts: 194

APPENDIX   C.

Fourth Order Band-Pass Filter Construction and Performance

MATLAB PROGRAM FOR THE DEVELOPMENT OF BAND-PASS FILTERS DEPICTED IN THIS DESIGN.

```
del th011a.met   % Meta file to contain output.
del th011b.met   % Meta file to contain output.
cls
clear
clg
w = 2*pi*200e3:500:2*pi*300e3;
s = j*w;
wt1 = 2*pi*15e6;              %Set the value of Unity Gain BW for the Op-amp
wt2 = 2*pi*15e6;
w01 = 2*pi*251760;
%w0 = (2*pi*254.6e3);         % enter w0
Q = 50;                % enter Q
R = 1000;                 % enter resistance
C = (R*w01)^(-1);
G = R^(-1);
A1 = wt1./s;
A2 = wt2./s;
Y1 = G;
Y2 = G;
Y3 = C*s;
Y4 = G;
Y5 = 0;
Y6 = G;
Y8 = C*s;
Y7 = G/Q;
J  = Y4+Y7+Y8;
K  = Y1+Y3;
L  = Y2+Y5+Y6;
%
NUM = ((K.*L.*Y7)./A1)+((Y2+Y6).*Y3.*Y7)+(Y1.*Y4.*Y5)...
     -(Y3.*Y5.*Y8);
DEN = ((J.*K.*L)./(A1.*A2))+((J.*L.*Y1)./A1)+((J.*L.*Y3)./A2) ...
     +((Y7+Y8).*Y2.*Y3)+((Y5+Y6).*Y1.*Y4);
T1 = (NUM./DEN);
T1a = sqrt((real(T1)).^2+(imag(T1)).^2);
%
R = 1000;                 % enter resistance
w02 = 2*pi*255760;
C = (R*w02)^(-1);
G = R^(-1);
```

```
A1 = wt1./s;
A2 = wt2./s;
Y1 = G;
Y2 = G;
Y3 = C*s;
Y4 = G;
Y5 = 0;
Y6 = G;
Y8 = C*s;
Y7 = G/Q;
J  = Y4+Y7+Y8;
K  = Y1+Y3;
L  = Y2+Y5+Y6;
%
NUM = ((K.*L.*Y7)./A1)+((Y2+Y6).*Y3.*Y7)+(Y1.*Y4.*Y5)...
    -(Y3.*Y5.*Y8);
DEN = ((J.*K.*L)./(A1.*A2))+((J.*L.*Y1)./A1)+((J.*L.*Y3)./A2) ...
    +((Y7+Y8).*Y2.*Y3)+((Y5+Y6).*Y1.*Y4);
T2 = (NUM./DEN);
T2a = sqrt((real(T2)).^2+(imag(T2)).^2);
x = [242.6e3 242.6e3 248.6e3 248.6e3];
y = [-5 7.2 7.2 -5];
plot(w/(2*pi),20*log10(T1a),w/(2*pi),20*log10(T2a),x,y);
title('Cascaded 2nd ORDER BP filters, Q=50');
xlabel('FREQ HZ');
ylabel('MAGNITUDE dB');
grid
meta th011a
T12 = T1.*T2;
T12a = sqrt((real(T12)).^2+(imag(T12)).^2);
plot(w/(2*pi),20*log10(T12a),x,y);
title('4th ORDER BPF, f0=245.76khz, Q=50');
xlabel('FREQ HZ');
ylabel('MAGNITUDE dB');
grid
meta th011b
```

Cascaded 2nd ORDER BP filters, Q= 50

4th ORDER BPF, f0= 245.76khz, Q=50

Desired bandwidth indicated by box 6 Khz

MAGNITUDE dB

FREQ HZ
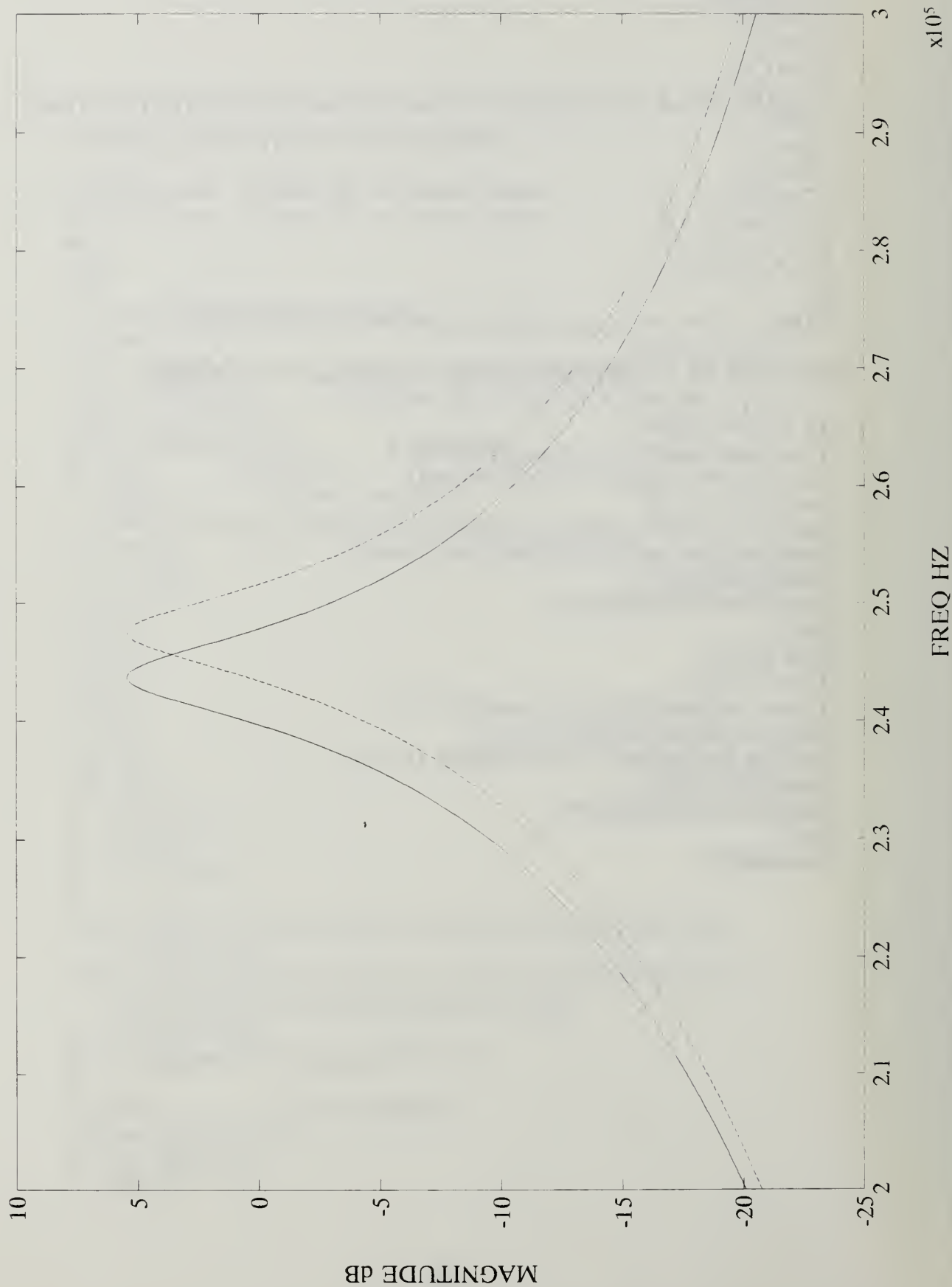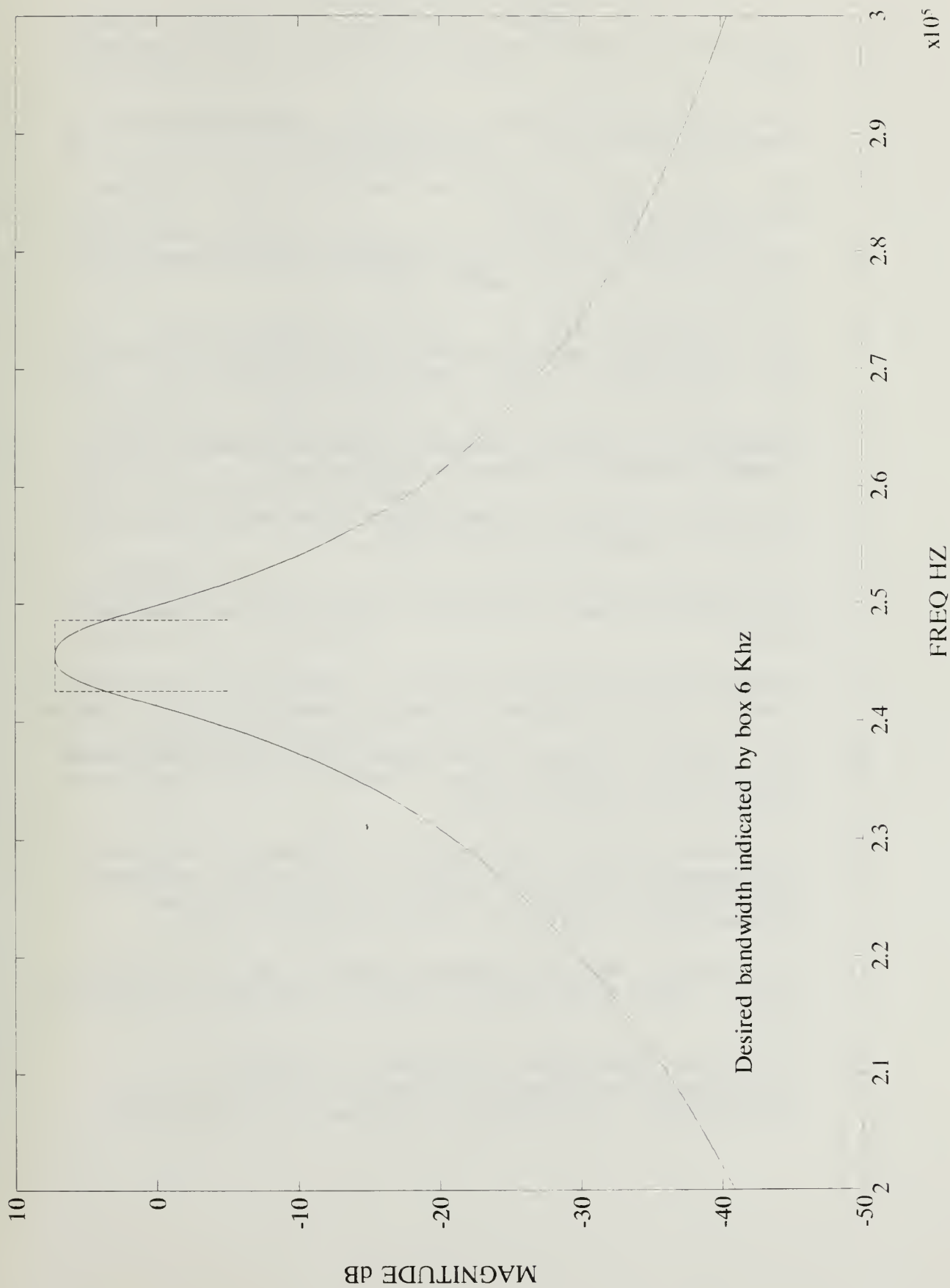
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